LISTA DE LUCRĂRI
Șef lucrări dr. ing. Ionel ZAGAN

4.a) Lista de lucrări (maximum 10 lucrări):

1. I. Zagan, V. G. Găitan, "FPGA implementation of hardware accelerated RTOS based on real-time event handling", The Journal of Supercomputing, Springer, 13 march 2023. https://doi.org/10.1007/s11227-023-05151-0, FI 2.557, zona Q2.
2. I. Zagan, V. G. Găitan, "Soft-core processor integration based on different instruction set architectures and field programmable gate array custom datapath implementation," in PeerJ Computer Science, PeerJ Comput. Sci. 9:e1300, 2023, http://doi.org/10.7717/peerj-cs.1300, FI 2.41, zona Q2.
3. I. Zagan, V. G. Găitan, "Custom Soft-Core RISC Processor Validation Based on Real-Time Event Handling Scheduler FPGA Implementation," in IEEE Access, vol. 11, pp. 36264-36280, 2023, https://doi.org/10.1109/ACCESS.2023.3266150, FI 3.9, zona Q2.
4. I. Zagan, V. G. Găitan, "Designing a Custom CPU Architecture Based on Hardware RTOS and Dynamic Preemptive Scheduler," Mathematics 2022, 10, 2637. https://doi.org/10.3390/math10152637, FI 2.4.
5. V. G. Găitan and I. Zagan, "Modbus Protocol Performance Analysis in a Variable Configuration of the Physical Fieldbus Architecture," in IEEE Access, vol. 10, pp. 123942-123955, 2022, doi: 10.1109/ACCESS.2022.3224720, FI 3.9, zona Q2.
6. I. Zagan, C-A. Tănase, V. G. Găitan, "Hardware Real-time Event Management with Support of RISC-V Architecture for FPGA-Based Reconfigurable Embedded Systems", Advances in Electrical and Computer Engineering, issue 1/2020, 29 Feb. 2020, FI 0.8.
7. I. Zagan, V. G. Găitan, "Real-Time Event Handling and Preemptive Hardware RTOS Scheduling on a Custom CPU Implementation," Canadian Journal of Electrical and Computer Engineering, Volume: 43, Issue: 4, October 2020, doi: 10.1109/CJECE.2020.3005360, FI 1.7.
8. I. Zagan, V. G. Găitan, "Hardware Scheduler Implementation based on Replicated Resource Architecture for Reconfigurable Systems", 2019 3rd International Symposiumon Computer Science and Intelligent Control (ISCSIC2019), 25-27 Sept. 2019, Amsterdam, Olanda.
9. I. Zagan, V. G. Gaitan, N. Iuga and A. Brezulianu, "m-GreenCARDIO embedded system designed for out-of-hospital cardiac patients", 2018 International Conference on Development and Application Systems (DAS), Suceava, Romania, 2018, pp. 11-17. doi: 10.1109/DAAS.2018.8396063.
10. I. Zagan, V. G. Găitan, "Implementation of nMPRA CPU Architecture based on Preemptive Hardware Scheduler Engine and Different Scheduling Algorithms", IET Computers & Digital Techniques, vol. 11, nr. 6, Noiembrie 2017, pp. 221-230, doi:10.1049/iet-cdt.2017.0163

4.b) Teza sau tezele de doctorat:

1. I. Zagan, "Contribuții la dezvoltarea sistemelor de operare în timp real cu funcții implementate în hardware", teză de doctorat susținută public în data de 22/06/2017, conducător științific Prof. univ. dr. ing. Vasile Gheorghiță GĂITAN.

4.c) Brevete de invenție:

1. Greensoft S.R.L., Gaitan V. G., Gaitan N. C., Geman O., Ungurean I., Petrariu A. I., Zagan I., Aghion C., Hăgan M. G., "Sistem de achiziție și procesare a parametrilor fiziologici", RO-BOPI 3/2020, 133934 A2, A61B 5/04, A61B 5/0402 din 30.03.2020.

4.d) Cărți și capitole în cărți:

1. I. Zagan, "Contribuții la dezvoltarea sistemelor de operare în timp real cu funcții implementate în hardware", ISBN: 978-973-666-513-4, Editura Universității "Ștefan cel Mare" Suceava, 2018.
2. V. G. Găitan, I. Zagan, "Rețele industriale locale – Modbus Extins", Editura Universităţii Ştefan cel Mare din Suceava, 2019, ISBN : 978-973-666-552-3

4.e) Articole/studii in extenso, publicate în reviste din fluxul ştiinţific internaţional principal:

1. I. Zagan, V. G. Găitan, "FPGA implementation of hardware accelerated RTOS based on real-time event handling", The Journal of Supercomputing, Springer, 13 march 2023. https://doi.org/10.1007/s11227-023-05151-0, FI 2.557, zona Q2.
2. I. Zagan, V. G. Găitan, "Soft-core processor integration based on different instruction set architectures and field programmable gate array custom datapath implementation," in PeerJ Computer Science, PeerJ Comput. Sci. 9:e1300, 2023, http://doi.org/10.7717/peerj-cs.1300, FI 2.41, zona Q2.
3. I. Zagan, V. G. Găitan, "Custom Soft-Core RISC Processor Validation Based on Real-Time Event Handling Scheduler FPGA Implementation," in IEEE Access, vol. 11, pp. 36264-36280, 2023, https://doi.org/10.1109/ACCESS.2023.3266150, FI 3.9, zona Q2.
4. I. Zagan, V. G. Găitan, "Designing a Custom CPU Architecture Based on Hardware RTOS and Dynamic Preemptive Scheduler," Mathematics 2022, 10, 2637. https://doi.org/10.3390/math10152637, FI 2.4.
5. V. G. Găitan and I. Zagan, "Modbus Protocol Performance Analysis in a Variable Configuration of the Physical Fieldbus Architecture," in IEEE Access, vol. 10, pp. 123942-123955, 2022, doi: 10.1109/ACCESS.2022.3224720, FI 3.9, zona Q2.
6. I. Zagan, C-A. Tănase, V. G. Găitan, "Hardware Real-time Event Management with Support of RISC-V Architecture for FPGA-Based Reconfigurable Embedded Systems", Advances in Electrical and Computer Engineering, issue 1/2020, 29 Feb. 2020, FI 0.8.
7. I. Zagan, V. G. Găitan, "Real-Time Event Handling and Preemptive Hardware RTOS Scheduling on a Custom CPU Implementation," Canadian Journal of Electrical and Computer Engineering, Volume: 43, Issue: 4, October 2020, doi: 10.1109/CJECE.2020.3005360, FI 1.7.
8. I. Zagan, V. G. Găitan, "Implementation of nMPRA CPU Architecture based on Preemptive Hardware Scheduler Engine and Different Scheduling Algorithms", IET Computers & Digital Techniques, vol. 11, nr. 6, Noiembrie 2017, pp. 221-230, doi:10.1049/iet-cdt.2017.0163

4.f) Publicaţii in extenso, apărute în lucrări ale principalelor conferinţe internaţionale de Specialitate:

1. I. Zagan, V. G. Găitan, "Hardware Scheduler Implementation based on Replicated Resource Architecture for Reconfigurable Systems", 2019 3rd International Symposiumon Computer Science and Intelligent Control (ISCSIC2019), 25-27 Sept. 2019, Amsterdam, Olanda.
2. I. Zagan, V. G. Gaitan, N. Iuga and A. Brezulianu, "m-GreenCARDIO embedded system designed for out-of-hospital cardiac patients", 2018 International Conference on Development and Application Systems (DAS), Suceava, Romania, 2018, pp. 11-17. doi: 10.1109/DAAS.2018.8396063.

Data: 15/01/2024

Ş.l. dr. ing. **Zagan Ionel**