

# Lista de lucrări

Dr. ing. Eugen Dodiu

Nr.	Titlu
<b>Teza sau tezele de doctorat</b>	
1	Teza Doctorat – “Planificator de timp real implementat hardware pentru sisteme embedded bazate pe FPGA”. Coordonator Științific: Prof.univ.dr.ing. Adrian GRAUR
<b>Brevete de invenție și alte titluri de proprietate industrială</b>	
2	Central Processing Unit With Banked Pipeline Registers, model utilitar înregistrat la Deutsches Patent und Markenamt, DE202012104250U1
<b>Articole</b>	
3	E. Dodiu, V.G. Găitan, “Custom designed CPU architecture based on a hardware scheduler and independent pipeline registers – concept and theory of operation”, 2012 IEEE EIT International Conference on Electro- Information Technology, Indianapolis, IN, USA, 6-8 Mai 2012, ISSN: 2154-0373, ISBN: 978-1-4673-0818-2, DOI 10.1109/EIT.2012.6220705
4	E. Dodiu, V.G. Găitan, A. Graur, “Custom designed CPU architecture based on a hardware scheduler and independent pipeline registers – architecture description”, IEEE 35'th Jubilee International Convention on Information and Communication Technology, Electronics and Microelectronics, Croația, 24 Mai 2012, ISBN 978-953-233-068-7
5	E. Dodiu, V.G. Găitan, și A. Graur, “Improving commercial RTOS performance using a custom interrupt management scheduling policy”, ACC'10 Proceedings of the 2010 international conference on Applied computing conference, Timișoara, Romania, 2010, pp. 61-66, ISSN: 1782-5808, ISBN: 978-980-474-236-3
6	E. Dodiu, A. Graur, și V.G. Găitan, “Hard-Soft Real-Time Performance Evaluation of Linux RTAI Based Embedded Systems”, Electronics and Electrical Engineering, Kaunas:Technologija, No.8(104), 2010, pp. 51-56, ISSN 1392-1215
7	N. C. Gaitan, V. G. Gaitan, St. Ghe. Pentiuc, I. Ungurean, E. Dodiu, “Middleware based Model of Heterogeneous Systems for SCADA Distributed Applications”, Advances in Electrical and Computer Engineering Vol 10, No 2, 2010, pp. 121-124, ISSN: 1582-7445 e-ISSN: 1844-7600
<b>Cărți</b>	
8	E. Dodiu, “Planificator de timp real implementat hardware pentru sisteme embedded bazate pe FPGA”, Editura Universității “Ștefan cel Mare” Suceava, ISBN 978-973-666-716-9

