Stefan cel Mare University of Suceava

Faculty of Electrical Engineering and Computers Science

Domain: *Electronics Engineering and Telecommunications*

Contributions to testing and characterization of electronic devices with applications in Large Hadron Collider (LHC) experiments

PhD Thesis

- Abstract -

Scientific coordinator:

Prof. Valentin POPA, *PhD*

Author:

Lucian-Nicolae COJOCARIU, Eng.

Doctoral guidance committee:

Prof. Mihai DIMIAN, *PhD*

Prof. Alin POTORAC, *PhD*

Prof. Aurelian ROTARU, *PhD*

~ SUCEAVA 2017 ~

Contents

List of abbreviations iii
General introduction 1
1. LHCb at CERN 3
1.1 LHCb detector architecture 4
1.2 RICH sub-detectors and photodetection system 5
1.3 The RICH Upgrade Program 6
2. Radiation effects in semiconductor devices 7
3. Multi Anode Read-Out Chip family 9
3.1 Test bench for the MAROC3 irradiation 9
3.2. Irradiation with X-Ray beam 11
3.3 Conclusions and originality 13
4. The Spatial Photomultiplier Array Counting and Integrating ReadOut Chip 15
4.1 Automatic test bench for irradiation 15
4.2 Irradiation test with 200 MeV proton beam 17
4.3 Conclusions and originality 20
5. Field Programmable Gate Array for High Energy Physics experiments 21
5.1 Heavy ions irradiation of KINTEX-7 22
5.2 Irradiation test with 200 MeV prtotons 24
5.3 Conclusions and originality 25
Conclusions and personal contributions 27

List of abbreviations

ADC	Analog to Digital Converter
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BRAM	Block Random Access Memory
CERN	European Organization for Nuclear Research
CLB	Configuration Logic Bloc
COTS	Commercial Off-The-Shelf
CRAM	Configuration memory
DAC	Digital to Analog Converter
DAQ	Data Acquisition
DD	Displacement damage
DRAM	Dynamic Random Access Memory
DUT	Device under test
EC	Elementary Cell
ECAL	Electromagnetic Calorimeter shashlik type;
FPGA	Field Programmable Gate Array
GBT	Giga-Bit Transceivers
GPIO	General-Purpose Input/Output
GUI	Graphical User Interface
HIF	Heavy Ion Irradiation Facility
HKMG	High K Metal Gate
HPD	Hybrid Photo Detector tube
I2C	Inter-Integrated Circuit interface
IC	Integrated Circuit
IFIN-HH	Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering
IT	Inner Tracker
JEM-EUSO	Japanese Experiment Module - Extreme Universe Space Observatory
JTAG	Joint Test Action Group interface
LET	Linear Energy Transport
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty

LS2	Second Long Shutdown
M_1 - M_5	Muon station
MaPMT	Multi Anode Photomultiplier tube
MAROC	Multi Anode Read-Out Chip
MBU	Multibit Upset
MOS	Metal Oxide Semiconductor
NIL	Non-Ionizing Energy Loss
OT	Outer Tracker
PCB	Printed Circuit Board
p-e	photoelectron
PSI	Paul Scherrer Institute
RICH	Ring Imaging Cherenkov detector
SBU	Single Event Burnout
SEE	Single Event Effect
SEFI	Single Event Function Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SEM IP	Soft Error Mitigation Core
SET	Single Event Transient
SEU	Single Event Upset
SiO_2	Silicon dioxide
SMPS	Switching Mode Power Supply
SPACIROC	Spatial Photomultiplier Array Counting and Integrating Readout Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
T_1 - T_3	Tracking stations
TID	Total Ionising Dose
TMR	Triple Modular Redundancy
TS	Tracking System
TT	Trigger Tracker
UART	Universal Asynchronous Receiver/Transmitter interface
USB	Universal Serial Bus interface
VELO	Vertex Locator system
VLSI	Very Large Scale of Integration

General introduction

Cutting edge applications in the area of wireless communications, broadband services, avionics, space stations and detectors for high-energy physics experiments relay on the state of the art semiconductor device. Following Moore's Law, the number of compact VLSI circuits obtained has increased as a result of the outstanding progress made in physics and production technology of semiconductor single crystals. The semiconductor devices impairment is driven by slight structural imperfections and insignificant concentration of impurities. In harsh environments, especially those with ionizing radiation, damages occur in the electro-physical properties of semiconductors.

Over time, many research groups carried out extensive studies meant to highlight the behaviour of electronic devices in the presence of ionizing radiations and the physical phenomena occurring due to the semiconductor irradiation. The progress achieved by the physics of radiation-resistant semiconductors allows us to design reliable electronic devices for extreme environments. The semiconductor device lifecycle strongly depending on the spectrum of particles and energy distribution for each radiation environment. Electronic devices experience radiation damages in environments like space, nuclear plants, high-energy physics experiments, including processing-induced radiation and natural environment.

High-Energy Physics Experiments, particularly those conducted on Large Hadron Collider (LHC) at CERN, demand electronic devices capable of reliable running into complex radiation field inside the collider tunnel as well as in detectors experimental. Therefore, a hostile environment for electronic devices is caused by a huge particle rate with a high intensity coming mostly from the primary hadron-hadron interaction and also from LHC machine material activation. The mixt radiation field at LHC consists on hadrons with wide energy spectra from 0.025 eV (thermal neutrons) up to hundreds of GeV. This represents a constant trouble for the electronics embedded into CERN accelerator complex infrastructure. The mixt-field radiation background inside LHC environment has two main sources. The first one is given by the proton-proton or lead-lead beams head-on collision inside detectors. The second one consists in distributed beam losses along the accelerator tunnel produced by interaction between protons and residual gas or materials surrounding the beam pipe.

In close proximity to the resulting accelerated beams are elements such as beam screens collimators, beam dump (point losses), cryostats, magnets and cables. All these materials interacting with a proton beam lead to hadronic cascade consisting of secondary particles as proton, neutron, pion, kaon, electron and positrons coming from a primary reaction. In turn, some of these particles possesses enough energy to contribute to the production of tertiary particles, this phenomenon can continue on if resulting particle have sufficient energy.

The main engineering constraint for the readout electronics and control systems in LHC accelerator complex is the radiation tolerance factor of semiconductor devices, these are Application Specific Integrated Circuits (ASIC) or selected from Commercial Off-The-Shelf (COTS) device market.

An Upgrade Programme is ongoing for the *Second Long Shutdown* (LS2) of LHC, starting in 2018 it will gave as main goal is to improve the LHC detectors performances. Some sub-detectors of the LHCb machine will be upgraded as well as both Ring Imaging Cherenkov (RICH) system which will be rebuild to run a beam bunch crossing rate of 25 ns. Their photo-detection system will be redesigned using electronic readout architecture COTS devices and radiation-hard by design ASIC's. For this was foreseen an irradiation hardness qualification campaign to evaluate the radiation tolerance of electronic device intended to be used in the RICH readout. The Romanian LHCb group got involved in this irradiation campaign by caring out tests on a front-end ASIC MAROC3 and for a Field Programmable Gate Array (FPGA)

from KINTEX-7 family of Xilinx. A third chip, SPACIROC2, was investigated due to the fact that its radiation-hard design is the blueprint for the next generation of MAROC family. Irradiation tests were performed with mono-energetic beams and the data analysis results are highlighted. Furthermore, for each chip the results are extrapolated to the LHCb detector nominal condition of radiation.

This thesis summarizes the work that has been done to evaluate the radiation tolerance of three integrated circuits, one implemented in a 28 nm high K metal gate (HKMG) and the other two are in 0.35 µm SiGe BiCMOS technology.

The first chapter provides an overview of the CERN accelerator infrastructure starting with a brief history of the organization and continuing with the physics program and four main experiments on the LHC ring. A detailed description of the LHCb detector is given, especially of the RICH sub-detector upgrade program. The new photo-detection system is presented together with the irradiation campaign for several integrated circuits radiations.

The second chapter introduces the concepts of radiation effects in a semiconductor device with a brief overview of the domain terminology. The effects induced by radiation are depicted, together with an outline regarding hardness techniques

The third chapter describes the MAROC3 chip architecture as well as the automated test benches designed and implemented for its radiation hardness qualification. Considered as a backup for the RICH photo-detection system front-end board, this integrated circuit is rad-hard by design and it was submitted for testing. Several samples were irradiated using a continuous X-ray spectra between 20-100 keV with a peak of 56 keV corresponding to the tungsten tube cathode. A dedicated section highlights the results of data analysis and interpretation.

The fourth chapter presents the SPACIROC2 chip architecture which serves as a blueprint for the next generation of the MAROC device family. This low power integrated circuit was designed for space applications to read out multi anode photomultiplier tubes on the Extreme Universe Space Observatory (JEM-EUSO). Inherited from MAROC3, the test bench was adapted for SPACIROC2 parameters online monitoring during irradiation tests. Its radiation tolerance was investigated with a 200 MeV proton beam and recorded data are presented and explained based on ASIC behaviour.

The fifth chapter is dedicated to the measure qualifying the radiation tolerance of an FPGA from KINTEX-7 family of XILINX. It was proposed as the main component for the digital communication board of the RICH read-out chain. A test board that respects the radiation hardness constrains was designed and implemented it inside the thinned dice of device under test. Data monitoring is accomplished by means of an automated test bench assembled to run in the irradiation vessel vacuum. The device was tested under beams of heavy ions and proton and the results of data analysis are shown.

1. LHCb at CERN

The European Organization for Nuclear Research houses a unique accelerator complex with four large experiments: ATLAS, CMS, LHCb and ALICE. A wide physics research program is ongoing and detectors gather huge quantity of data from colliding protons or heavy ions. Exploiting the Large Hadron Collider capabilities at full potential and improving detectors data taking will be possible after the Third Long Shutdown in 2025.

After the first Long Shutdown (LS1) ending in 2014, the LHC machine was upgraded to its nominal colliding energy of 14 TeV. Currently, the CERN accelerator complex, schematically represented in figure 1-1, consist of six accelerators and one decelerator.

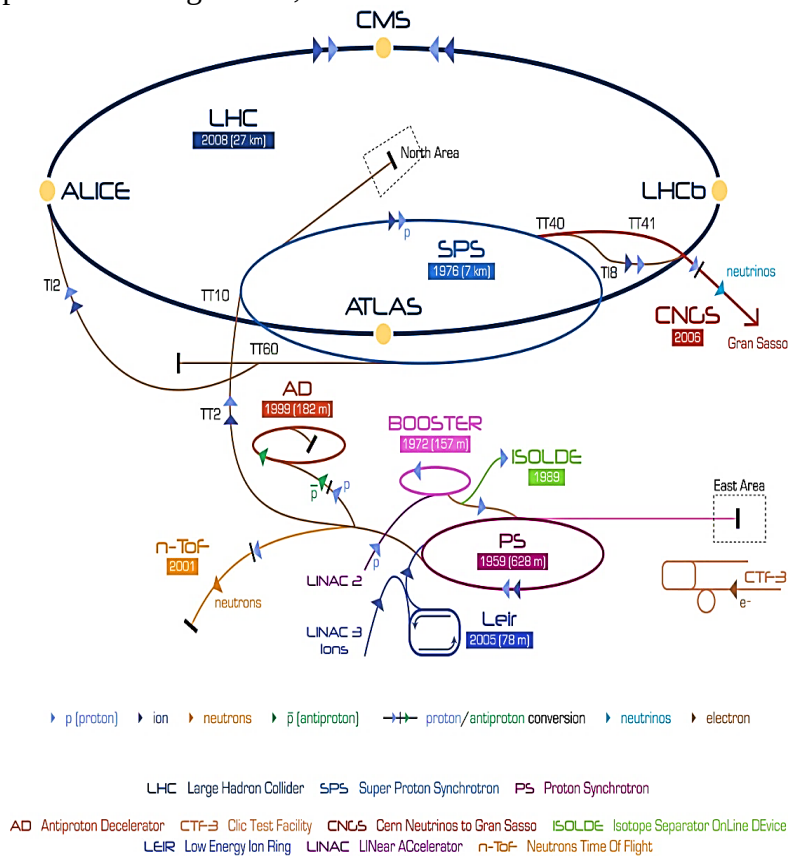

Figure 1-1 The CERN accelerators complex.

There are four interaction points, on the two rings from the LHC machine accelerator, associated with four large experiments that have the following acronyms: ATLAS (A Toroidal Large Hadron Collider Apparatus), CMS (Compact Muon Solenoid), ALICE (A Large Ion Collider Experiment) and LHCb (Large Hadron Collider beauty).

The LHCb is an experiment at LHC with the purpose of searching the new physics by indirect evidence in the Charged-Parity (CP) violation mechanism along with precise measurements of beauty and charm hadrons rare decays. A particularity in distinguishing the heavy flavour hadron from the background consists in their large lifetime, such as a 1.51 ps for B and a 0.41 ps for D^0. Such particles have a flight distance of a couple millimetres in most of the decay instances, as result of their large boost production in conjunction with lifetime.

Observing the decay of such particle allows a deep perception into the matter structure and the forces governing the sub-atomic constituents. One year of data taking at LHCb, with luminosity of $2x10^{32}$ $cm^{-2}s^{-1}$, means around 10^{12} pair of bb will be produced in 10^7 s of the

facility's total running time. The first advantage of running the LHCb detector at this modest luminosity is motivated by the events occurring as result of single proton-proton interaction per bunch crossing. In consequence, the data are simpler to analyse compared to the situation where multiple primary proton-proton interactions are taking place. Beside this, at low luminosity the radiation damage is reduced in the subdetectors front-end electronics operating close to the interaction point or beam pipe.

1.1 LHCb detector architecture

The experiment takes advantage of a detector architecture acting as a single-arm spectrometer with a forward angular acceptance starting from 10 mrad up to 300 mrad in the bending plane, while in the non-bending from 10 mrad to 250 mrad. Located in Point 8 of the LHC, the LHCb detector has a geometry made of sub-detectors specialized in particles identification, trajectory reconstruction and momentum measurements. The LHCb detector cross-section view is presented in figure 1-2 assigning the right-handed coordinate system with a z axis along the beam pipe and the y axis along the vertical.

In the non-bending y-z plane is showed the warm diplo magnet, the beam pipe as well as the sub-detectors part of Tracking System (TS) and Particle Identification System. Detailed, the LHCb parts are:

- VELO – the Vertex Locator system, including a pile-up veto counter;
- TT – trigger tracker;
- T_1, T_2, T_3 – tracking station consisting of Outer Tracker (OT) and Inner Tracker (IT);
- RICH1, RICH2 – Ring Imaging Cherenkov sub-detectors;
- SPD, PS – Scintillator Pad Detector and Preshower;
- ECAL – Electromagnetic Calorimeter shashlik type;
- HCAL – Hadronic Calorimeter;
- M_1, M_2, M_3, M_4, M_5 – muon detection system.

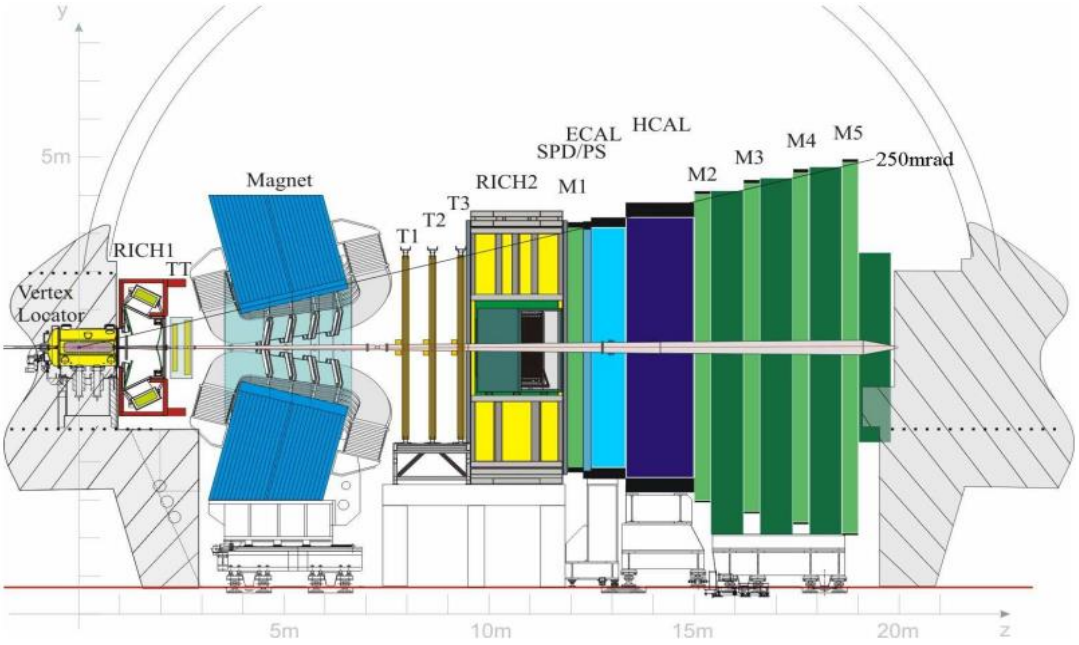

Figure 1-2 The cross-section of LHCb detector.

1.2 RICH sub-detectors and photodetection system

An essential key in the high-energy physics program at LHCb is the ability to provide particle identification for b hadron decays. The final state particles are pions, kaons and protons, in case of these decays. Particle identification is carried out combining the particles velocity measurements with the momentum information, allowing further the mass calculation of individual particles. The tracking system measures the particles tracks curvatures in the magnetic field and, therefore, their momentum. For velocity measurements, the Ring Imaging Cherenkov detectors (RICH) are used, basing their principle of operation on the Cherenkov radiation. The Cherenkov effect is given by charged particles that passes through dielectric material with a speed greater than the phase speed of light in the same medium and photons are emitted.

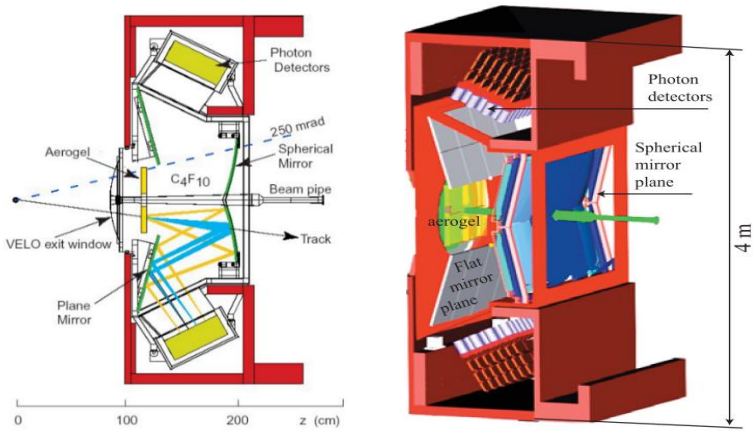

Figure 1-3 The RICH1 sub-detector architecture presented in cross section (on the left) and 3D (on the right).

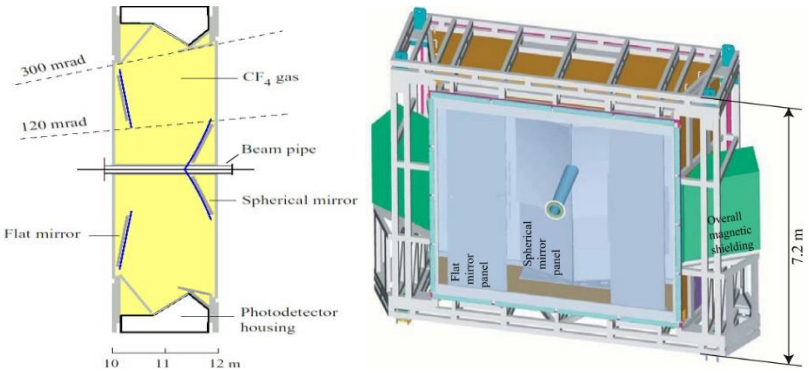

Figure 1-4 The RICH2 sub-detector architecture view from the top (on the left) and its 3D representation (on the right).

The LHCb detector used in the particle identification system has a chain of two RICH sub-detectors to fully cover a momentum range from 1 GeV up to 150 GeV. RICH1 as well as RICH2 rely on the same working principal, design and technology. The Cerenkov photons emitted in a cone, when charged hadrons pass through the radiator, are focused with spherical mirrors and reflected using flat mirrors on photodetectors planes situated beyond the LHCb acceptance. Both sub-detectors are equipped, individually, with two planes of photodetectors. RICH1 has the photodetectors plans placed above and below the beam pipe, see figure 1-3, while in the RICH2 are situated on the side of the beam pipe, see figure 1-4. The Cerenkov

photons in the RICHs sub-detectors chain are collected using large areas of photodetectors planes equipped with Hybrid Photo Detector tubes (HPD).

1.3 The RICH Upgrade Program

Foreseen to start in 2018, the RICH Upgrade Program involve the photodetection system redesign. The Cherenkov photon detection will be implemented using a commercial baseline with Multi Anode Photo Multiplier Tubes (MaPMT). All semiconductor devices part of the MaPMTs readout, either from front-end boards or digital boards, must withstand to mixt-radiation field inside LHCb detector. The photodetection planes, occupied by MaPMTs, will benefit from read-out electronics running with 40 MHz LHC clock. A preliminary version of its general architecture for the read-out system is presented in figure 1-5.

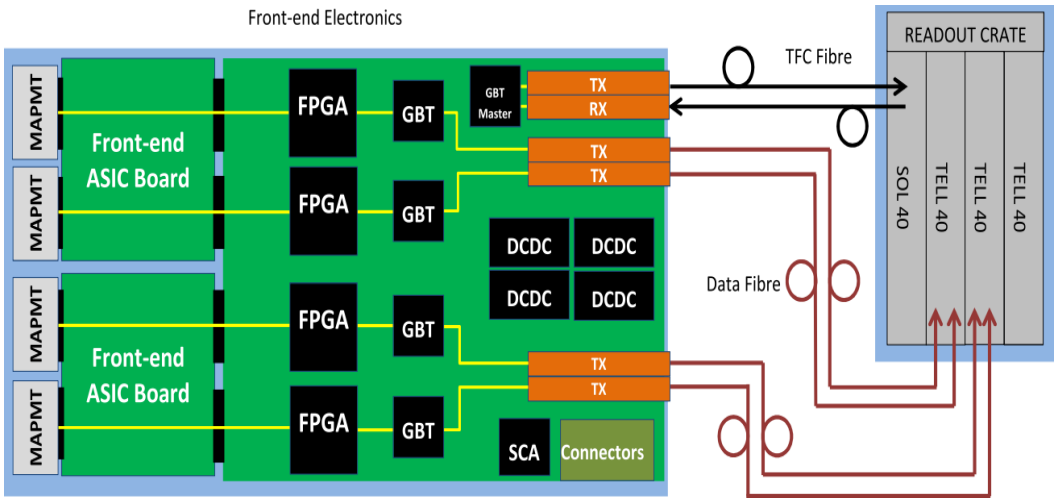

Figure 1-5 Read-out electronics chain for RICH subdetectors new photodetection system and TELL40s.

The front-end boards discriminate the signals generated by the MaPMTs and the output data, delivered by front-end ASIC, will undergo format procedure for the GBT transmission protocol requirements. Further, the data are sent over optical links in the counting room where TELL40 modules receive them. The porpoise of TELL40 FPGA based module is to handle data coming from each subdetector to the computer farm. Finally, the data readout from both RICH subdetectors is delivered to the computer farm, which in the end performs event reconstruction, data filtering and storage.

2. Radiation effects in semiconductor devices

In LHC experiments proton bunches collides head-on at every 25 ns leaving behind a harsh radiation environment. High energy physics detectors, avionics, space probes, military applications demand radiation tolerant electronics meant to have a reliable operation in environments with radiation. Various types of radiation induced effects can occur in a device semiconductor lattice, thus depending on the type of particle passing through and its kinetic energy. These effects are classified in two groups. The first one, represented by cumulative effects, appears gradually because of accumulated radiation dose on time. Second group, Single-Event Effects (SEE), can be triggered by just a single highly ionizing particle producing a very large local change deposit in semiconductor layers.

A comprehensive view upon each radiation effect presented in figure 2-1 it will be presented in detail over present chapter.

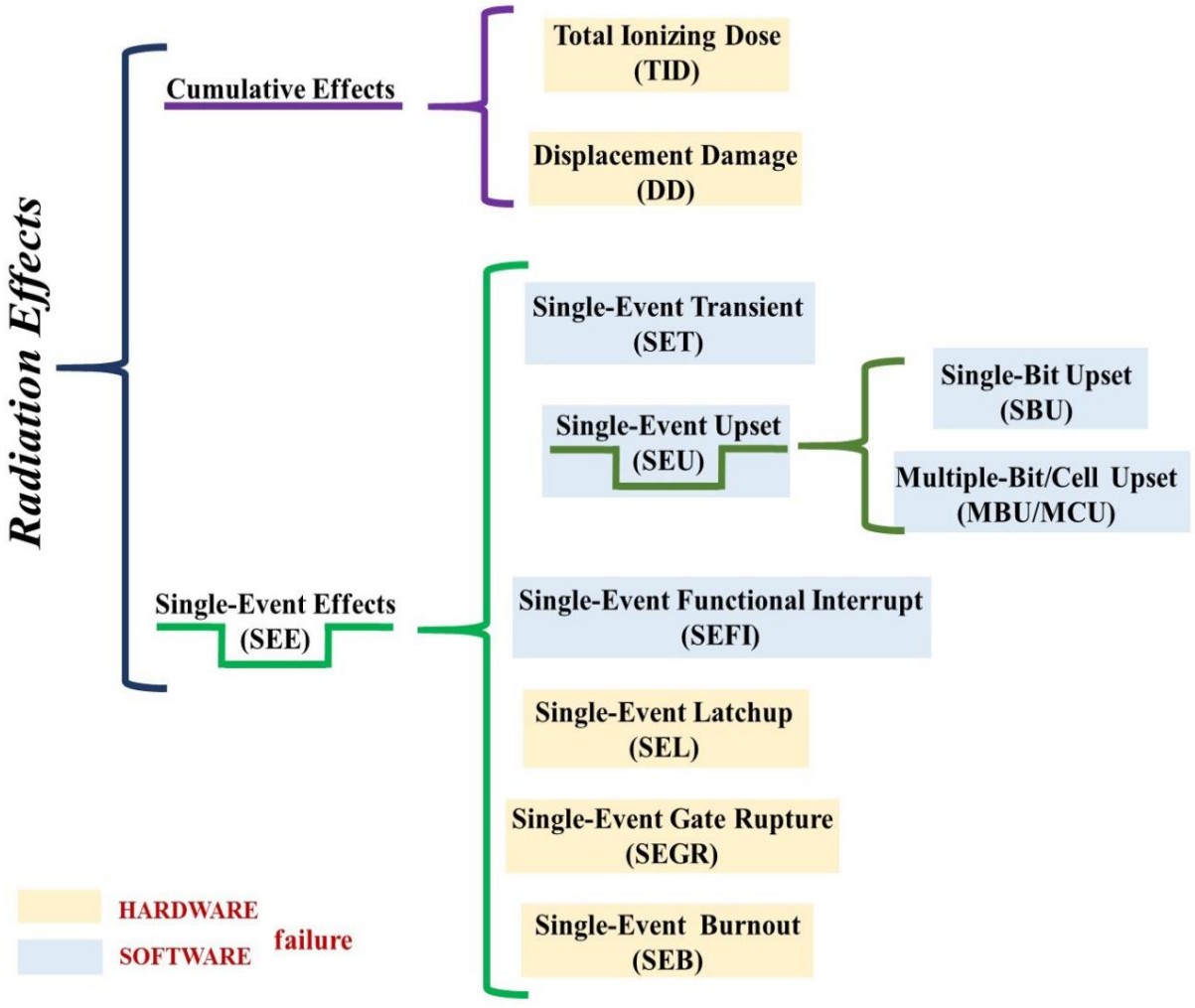

Figure 2-1 Radiation-induced effects into semiconductor devices.

Non-ionizing energy loss (NIEL) is physical process driven by the energy loss of particles through a material resulting in permanent atomic displacement. The NEIL ions could interact with nuclei and not with atomic electrons. This interaction could be elastic or inelastic, for inelastic interaction resulting residuals nuclei, protons and neutrons(nucleons).

Displacement damage (DD) is produced mainly by neutral particles, as example neutrons, leading mostly to an atom displacement or even to an avalanche of displacements in to the device semiconductor lattice.

The total ionising dose (TID) affects mainly the MOS devices in a more distinct way influencing both substrate and insulating layer proprieties through the trapping centres formation and interface states.

Single Event Transient (SET) is a fleeting disturbance in voltage or current following immediately particle strike on the semiconductor lattice.

Single Event Upset (SEU) phenomena leads to changes in logical state or transient disruptions latch as valid signals in semiconductor memory cel, hence a bit flipped.

Multi Bit Upset (MBU) is caused by a single high energetic particle that trigger multiple upsets within memory cells either SRAM or DRAM and other semiconductor based storage technology.

Single Event Function Interrupt (SEFI) phenomenon emerge within complex integrated circuits and manifested itself through a disruption of device operation after a sensitive volume of its architecture was strike by a single high energetic particle.

Single Event Latchup (SEL) leads to a regenerative current flow condition triggered by two cross-coupled parasitic bipolar transistors forming a semiconductor controlled rectifier (SCR), therefor a low resistance path between power supply rail, when an energetic particle strike the device and deposit enough charge to turn ON the parasitic structure.

Single Event Gate Rupture (SEGR) triggers in the MOS transistors a localized breakdown of the dielectric material when a single energetic heavy-ion strikes the gate region.

Single Event Burnout (SEB) is a complete damage mechanism especially encountered in both power MSOFET and bipolar power transistors when are exposed to heavy ions, energetic neutrons and protons.

3. Multi Anode Read-Out Chip family

The CNRS-IN2P3-Ecole Polytechnique microelectronics design centre or shortly the OmegaMICRO developed a wide range of font-end ASICS dedicated to detectors and sensors in the experimental field of astrophysics, particles and nuclear physics plus medical imaging. One of these is the Multi Anode Read-Out Chip (MAROC) family developed for the MaPMT read-out or similar photodetector technology. In the context of LHCb Upgrade Program, the MAROC3 was a backup solution for the front-end read-out of the two RICH sub-detectors.

The MAROC3 chip was implemented in a AMS SiGe 0.35 µm technology with a power consumption of 3.5 mW/channel, see its architecture layout in figure 3-1. This ASIC is dedicated mainly to read-out the MaPMT's 64 channels. In terms of design features, MAROC3 was implemented to: correct channel to channel gain spread of MaPMT; generate 64 trigger signals corresponding to the 64 photomultiplier tube anodes; processes with a 100% trigger efficiency input signals starting from 50 fC (1/3 photo-electron equivalent) up to 1.6 pC; having channels cross talk of 1% and noise of 2fC.

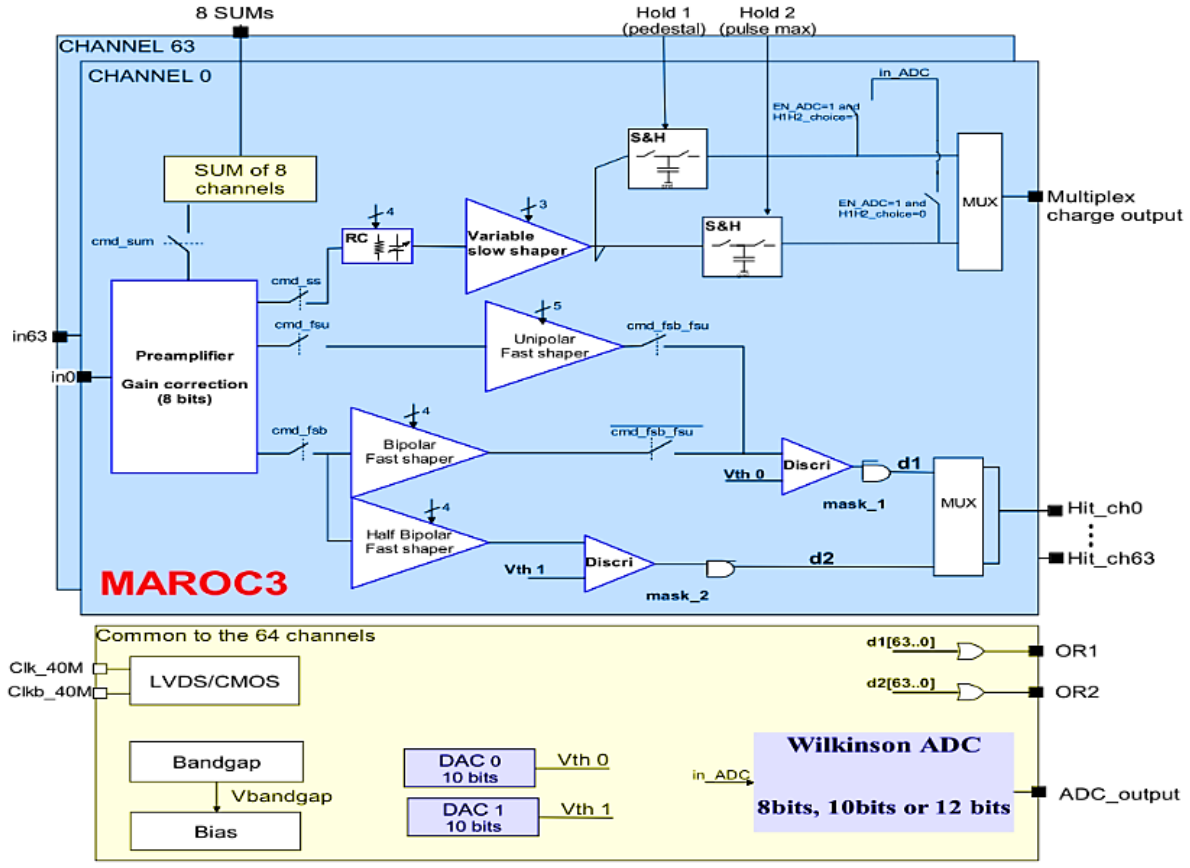

Figure 3-1 Layout of MAROC3 front-end ASIC architecture.

3.1 Test bench for the MAROC3 irradiation

In preparation for the MAROC3 radiation hardness qualification procedure for the RICH subdetectors mixt-field radiation environment, the parameter nominated to be monitored were established jointly by the LHCb Romanian Group with the ASIG design team. The adopted procedures entail to monitor the MAROC3 parameter listed in table 3-1. After each irradiation

dose, the parameters are checked again. There is a list of parameters to be monitored before and after each deposited radiation dose and a second that should be recorded online during the dose deposition. Later analysis of each below recorded parameter might highlight signs of radiation induced effects. By correlating the monitored parameters evolution in time, it is possible to distinguish among various type of effects and to isolate functional parts of the chip where they occur.

Table 3-1 List of monitored parameters in MARO3 radiation hardness study

before /after irradiation	during irradiation
• DAC's linearity	▪ Threshold voltage
• S curves for all channels	▪ Chip power consumption
• Chip power consumption	▪ ASIC internal voltage reference (Vbandgap)
• ASIC internal voltage reference (Vbandgap)	▪ DC voltage component of Slow/Fast Shaper
• DC voltage component of Slow/Fast Shaper	▪ Chip and PCB Temperature
• Chip and PCB Temperature	

Monitoring the parameters and gathering data during irradiation tests is taking in to account that the data acquisition (DAQ) system and other electronic equipment must be far away from the device under test (DUT), in this case MAROC3 chip. Therefore, all the wires connected to the DUT board are detached in two and equipped with connectors matching the one mounted on the vacuum vessel. The users oversee and operate everything from the control room. I proposed and implemented an automatic test bench for the MAROC3 radiation hardness assessment appropriate for heavy ions, proton, neutron and X-ray irradiation testing facilities. The MAROC3 automatic test bench has the design layout presented in the figure 3-2.

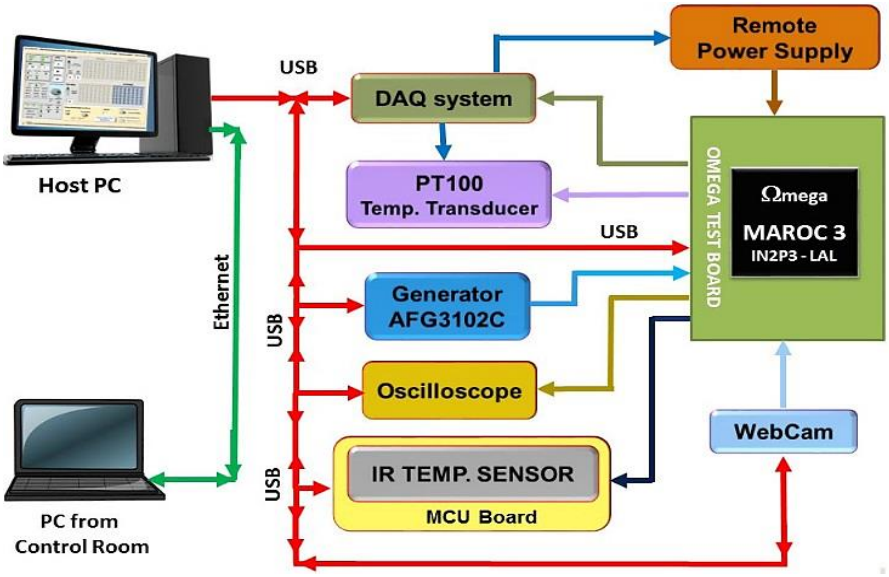

Figure 3-2 Test bench architecture for MAROC3 online monitoring.

Each of the test bench equipment is connected to the host PC over USB interface and further the user has access to the collected data via Ethernet from the control room PC. The DUT board is powered through a shielded multicore cable 4 m long from a remote-controlled power supply unit custom made. The pulse generator along with the oscilloscope are dedicated to be used in Scurve tests. With the help of an AFG3102 generator the MaPMT signals are emulated, maintaining a constant input charge for all 64 analog channels of the DUT. The signals are checked by the oscilloscope. As DAQ system, a commercial based solution with NI DAQ6009 was chosen. The power supply is connected to the DAQ system that enables/disables its output rails.

3.2. Irradiation with X-Ray beam

A first look to the MAROC3 radiation tolerance was made by means of the X-Ray radiation facility available at the Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH). The entire X-Ray irradiation setup is presented in figure 3-3. Profile for the 56 keV X-Ray beam has a fan shape of 80°x10°. The MAROC3 test board was placed at 10 cm in front of the monoblock surface and in between a 5 mm lead mask was installed. This ensured radiation protection for the rest of electronic devices populating the DUT board, while the MAROC3 chip was irradiated through a 5 cm square aperture. The infrared contactless temperature sensor was used only to check from time to time the temperature in the dice. In the right side of figure 3-3 all these elements can be seen.

All electronic monitoring and control programming equipments were put away from the X-Ray source, part of them can be seen in the left side of figure 3-3. The test bench was remote controlled from another room. The irradiation procedure was initiated considering the following preliminary doses: 40 krad, 400 krad, 1 Mrad, 2.5 Mrad.

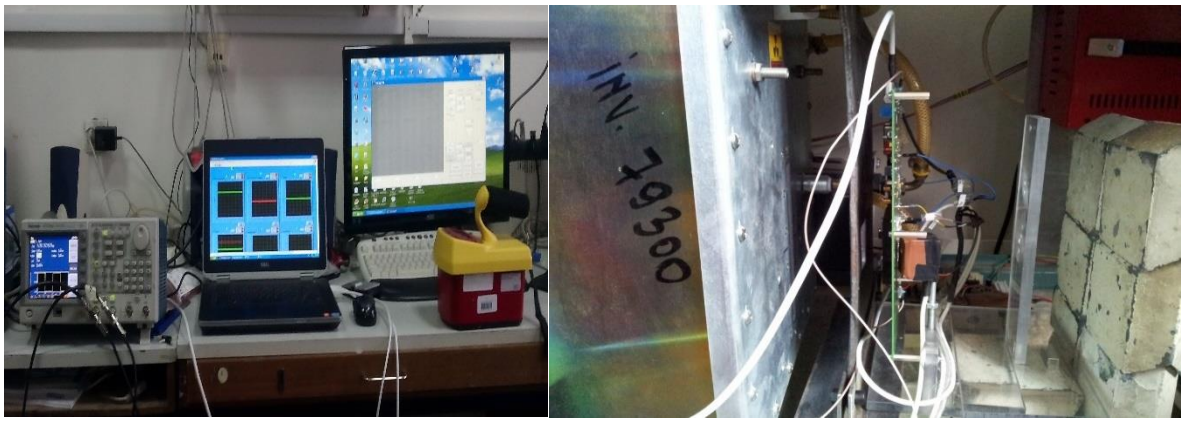

Figure 3-3 The MAROC3 test bench installed into X-Ray generator.

Prior to the X-Ray irradiation two MAROC3 chips were characterised extensively in the laboratory from electrical parameters stand point. The electrical parameters recorded were kept as baseline. After test bench installation at irradiation site, each chip was monitored for 30 minutes on irradiation place close to the X-Ray machine. For each deposited dose, I done a complete set of measurements in compliance with the list of parameters in the table 3-1. Data analysis was performed for both chips in detailed and since both chips had rather the same behaviour in the beam. No sudden changes within the MAROC3 monitored parameters occurred during irradiation test. Temperature inside the X-ray generator enclosure increase from 21 ^{0}C to 29 ^{0}C, see figure 3-7, and this is due to the heat dissipation on tungsten filament

of X-ray tube and from other machine elements. After the pick of 29 ^{0}C the temperature inside enclosure decrease slightly because of the diurnal temperature.

A closer introspection of the chip parameters proved that the DUT supply voltage did not suffer any considerable variation, while the chip current consumption rise with 1.5% at the end of the 2.5 Mrad dose. No sign of SEL can be seen in the current consumption trend. The DAC0 output voltage, stays linear for each dose and no local fluctuations took place. The DAC linearity curves which overlaps perfectly down to 0.9 V (DAC register value 650) to the one measured before applying the first X-Ray dose. Further down to 0 V the curves stars to deviate for one or another barely. The Bandgap voltage reference curves, start to decrease at 2.5 Mrad, however the fluctuation is less than 2%. Other parameters such as the DC component of the Slow Shaper, or that of the Fast Shaper did not show any significant variation.

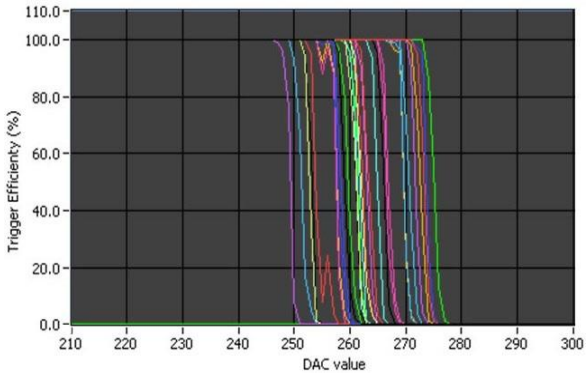

Figure 3-4 The MAROC3 efficiency curves before irradiation.

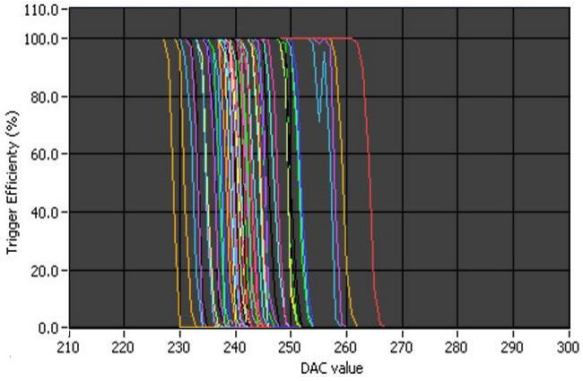

Figure 3-5 The MAROC3 efficiency curves after 1 Mrad X-Ray dose.

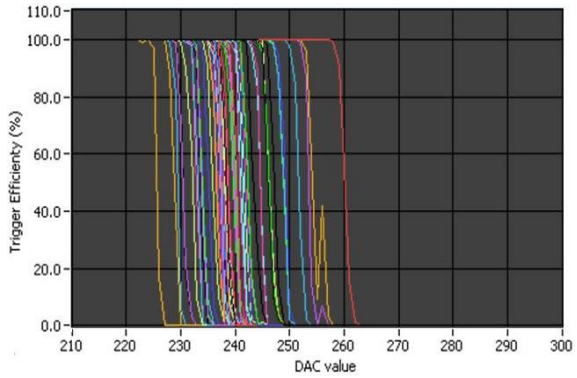

Figure 3-6 The MAROC3 efficiency curves after 2.5 Mrad X-Ray dose.

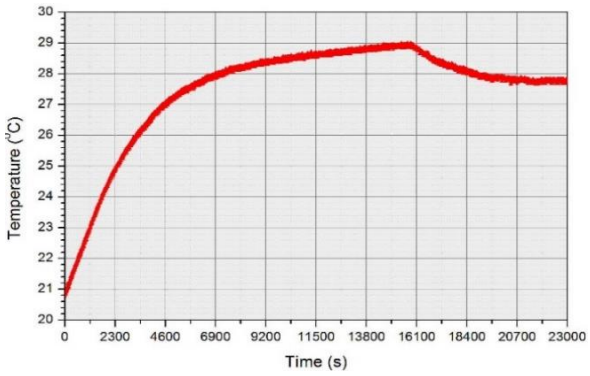

Figure 3-7 Temperature variation within X-Ray machine enclosure during the test.

The S-curve graphs (trigger efficiency curves from figure 3-4 to 3-6) were determined before and after each applied dose of radiation. A fix charge of 150 fC was applied to all 64 analog channels of the MAROC3. The results highlight, from dose to dose, a shifting trend of the Scurves. Even so the chip behaved well within the range considering the high dose applied. After irradiation, the two MAROC3 chips were again tested in the laboratory and only insignificant changes were observed on monitored parameters and even these are probably due to temperature changes rather than TID. Overall, the MAROC3 proved to be stable during running at this high X-ray TID value. Still, a dedicated thermal study must be carried out to better understand how the chip parameters changes with the temperature, especially for the environment with considerable temperature fluctuation.

3.3 Conclusions and originality

The Romanian LHCb group accomplished the first irradiation test of an MAROC3 chip by evaluating its radiation tolerance against the TID with 56 keV X-ray beam. Further, irradiation tests with protons and heavy ions are foreseen. This preliminary test with X-ray is the starting point of the irradiation campaign planned for the MAROC3. Also, its vulnerability to various SEE must be carefully checked. It is mandatory for the chip to be immune to SEL for heavy ions with LET below 15 MeV cm^2/mg while the LET threshold is desirable to be as high as possible preferably above 70 MeV cm^2/mg. Likewise, the chip tolerance to proton beams with energy above 20 MeV will be mandatory. Again, the final dose will be 8 Mrad for the TID and a higher proton beam energy will rise the probability for DD and SEE to occur. Therefore, the possibility of permanent effects induced by protons must be investigated.

Close collaboration with the OmegaMICRO developer helped me to develop a viable monitoring strategy for the chip as well as a deeper understanding of its operation. In this context, I proposed and implement an automated test bench for MAROC3 monitoring under irradiation. Other knowledge was passed to us by other LHCb group involved in the testing of CLARO radiation tolerance, also a MaPMT read-out ASIC.

The developed test bench proved reliable over many hours of testing, but the DAQ system did not fit our requirements. Most probable, a better custom DAQ system will be implemented for upcoming tests and this will surely have anti-aliasing filters and voltage buffers upon each channel. Despite the fact that we used only shielded cable, usually 4 m long, we must account for its influence on the sampling noise for the future DAQ system.

4. The Spatial Photomultiplier Array Counting and Integrating ReadOut Chip

The SPACIROC2 chip acronym stands for Spatial Photomultiplier Array Counting and Integrating Readout Chip, see its architecture layout presented in figure 4-1. This is a front-end ASIC developed for the MaPMT read-out and its mainstream application is to equip detectors in the Japanese Experiment Module (JEM) on the International Space Station (JEM-EUSO) space observatory dedicated to the study of extremely high-energy cosmic rays. The SPACIROC prototype is also a blueprint for the next generation of MAROC, desired to be more radiation tolerant.

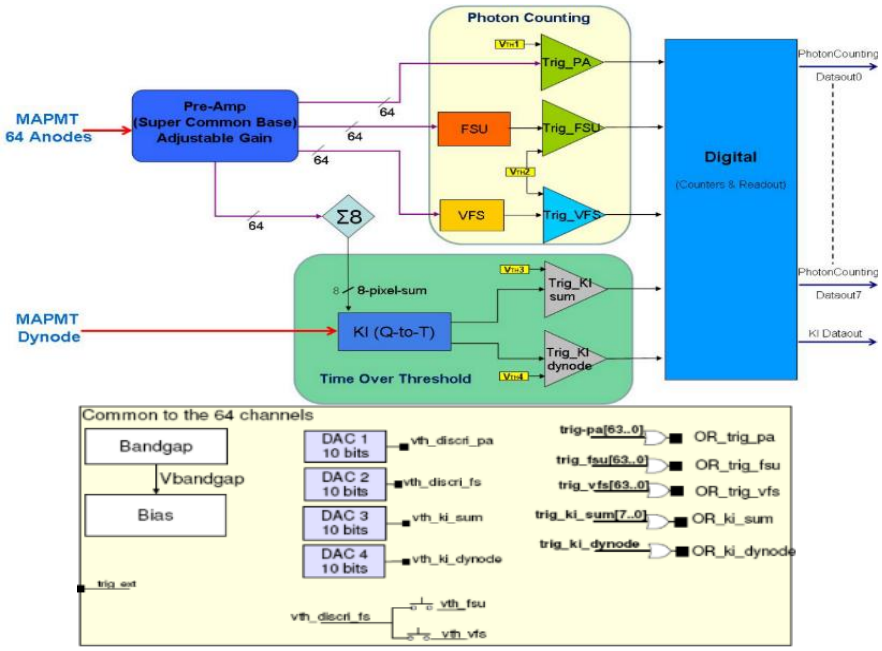

Figure 4-1 General architecture of SPACIROC2 chip.

Implemented within 0.35 µm SiGe BiCMOS technology at the Austria Micro System Company, the SPACIROC2 is a prototype ASIC with the following features: a low power consumption of 1mW per channel; 100% trigger efficiency for an input charge starting at 50 fC (1/3 photo-electron) with a 30 ns double pulse resolution; charge to time (Q-to-T) converter from 2 pC up to 400 pC; a MaPMT gain spread correction with a 64 channels preamplifier that allows each individual channel gain adjustments on a 8-bit resolution.

4.1 Automatic test bench for irradiation

Similarly, the parameters to be monitored during tests were initially discussed with the SPACIROC design team. This time a more extensive list of parameters to be monitored and measured before, during and after irradiation qualification test is given in table 4-1. Three test boards equipped with SPACIROC2 chips were carefully investigated in normal condition from the electrical parameters stand point and not only. The DAC2 linearity test will highlight if this mixt signal circuitry is susceptible to the cumulative effects caused by the TID or permanent damage induced by SEEs like SEGR. Any malfunction of the digital part in conjunction with the Photon Counting unit will manifest in the S-curve and pedestal alterations.

Table 4-1 List of the monitored parameter for SPACIROC2

before /after irradiation	during irradiation
• Test board power consumption	▪ Test board power consumption
• ASIC analog part power consumption	▪ ASIC analog part power consumption
• ASIC digital part power consumption	▪ ASIC digital part power consumption
• DAC2 linearity	▪ Internal voltage references (Vbandgap)
• Internal voltage references (Vbandgap)	▪ DC voltage component of Analog Probe (PA_BUFF)
• DC voltage component of Analog Probe (PA_BUFF)	▪ DAC1 output (vth_discri_pa)
• DAC1 output (vth_discri_pa)	• DAC1 output (vth_discri_pa)
• DAC2 output voltage (vth_discri_fs)	• DAC2 output voltage (vth_discri_fs)
• DAC3 output voltage (vth_ki_sum)	• DAC3 output voltage (vth_ki_sum)
• Trigger efficiency Scurve	• Temperature
• Pedestals	
• Temperature	

I proposed and contributed to the implementation of an automatic test bench used for the ASIC radiation hardness qualification procedure, all this being possible with support from OmegaMICRO researchers. The hardware layout is shown on the left side of figure 4-2. The innovative components of the test bench hardware are the data acquisition (DAQ) system and the remote-controlled switching mode power supply (SMPS).

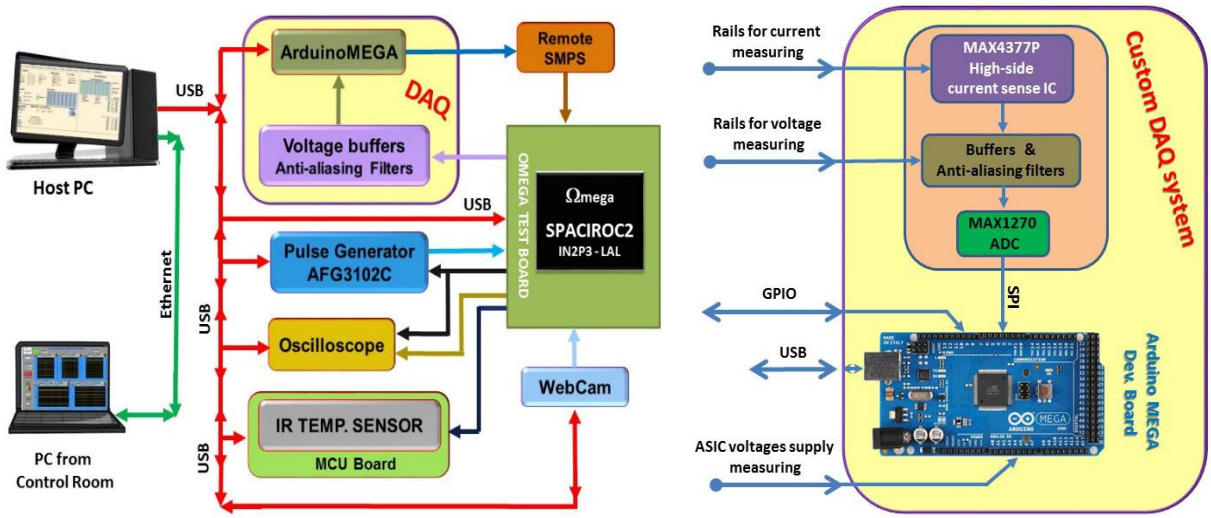

Figure 4-2 Layout of the automatic test bench for SPACIROC2 under irradiation (left side) and the data acquisition system architecture (right side).

The custom DAQ features are: 24 analogue inputs of which 16 on 10-bit resolution and 8 on 12-bit resolution; 54 digital GPIO connectors; high-side current sense amplifiers; analogue voltage buffers and anti-aliasing filters. The processing unit of the DAQ system is built around a commercial Arduino Mega development board. The 8 analogue inputs with 12-bit resolution are read through an external MAX1270 ADC connected to the processing unit via a SPI interface. Four out of the ADC inputs are dedicated to the high-side current sense amplifiers from the MAX4377 series. The signal conditioning block has the voltage buffers implemented

with unit gain stabile operational amplifier MCP6424 followed by a network of RC passive anti-aliasing filters. All analogue voltage inputs pass through the signal conditioning block and goes in the ADCs. The MaPMT signals are produced by a pulse generator synchronised to the SPACIROC2 test board output signal. Except the SMPS, all the test bench components communicate the measured data via a USB interface to a host PC placed at a safe distance inside the irradiation room. This data is then forwarded over Ethernet to the PC from the control room operated by the technicians managing the tests.

4.2 Irradiation test with 200 MeV proton beam

The first test in the SPACIROC2 irradiation campaign was carried out at the Proton Irradiation Facility (PIF) from Paul Scherrer Institute (PSI), Switzerland. In the case of SPACIROC2, a 200 MeV proton beam was used with a flux of $1.089 \cdot 10^9$ protons/cm^{2}s. The DUT board was mounted on a metallic sampler holder in front of the beam exit window along with the test bench as it can be seen in figure 4-3. A laser alignment procedure was used to properly position the 19 mm^2 (4.6 mm x 4.1 mm) chip die with respect to the beam axis. A full test has been done of each DUT after being installed on the beam line and before the beam was active. The measured values for the parameters were qualitatively checked against the baseline values taking into account the temperature inside the irradiation room which varied in the range 30-36 ^{0}C.

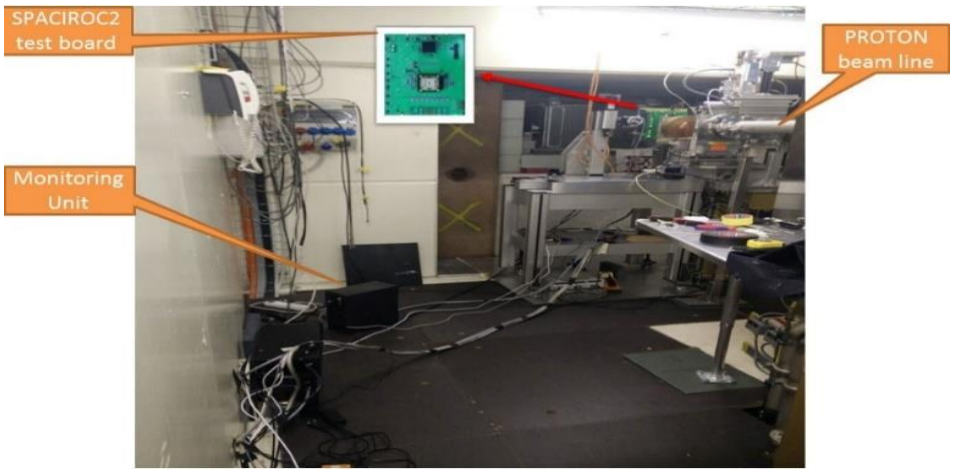

Figure 4-3 The SPACIROC2 test bench installed at PIF (left side) and the beam line in close view (right side).

Three SPACIROC2 samples was irradiated up to 100 krad TID (Si) each. All three ASIC samples did not show any significant variation during irradiation for the following parameters: internal voltage reference ($V_{bandgap}$), DC voltage component of Analog Probe (PA_BUFF), DAC1 output, DAC3 output and DAC2 output. With the purpose of determining the TID threshold where the chip ceased to run properly, the irradiation was pursued in steps of 10 krad up to 100 krad. For the final TID of 83.12 krad a step increase is observed within analog bloc power consumption. Two high current states of the digital block were registered as for the first chip. The SELs occurred at TIDs of 14.78 krad and 67.72 krad and the chip functionality was recovered with power cycles - see figure 4-4. The digital block current started to grow in steps at around 60.72 krad. During the last exposure to the proton beam, the board was power cycled four times, as shown in figure 4-5, but the current in the digital block did not return to its

baseline value. Only after annealing at room temperature the TID effects disappeared and the current consumption on the chip digital rail returned to its reference level.

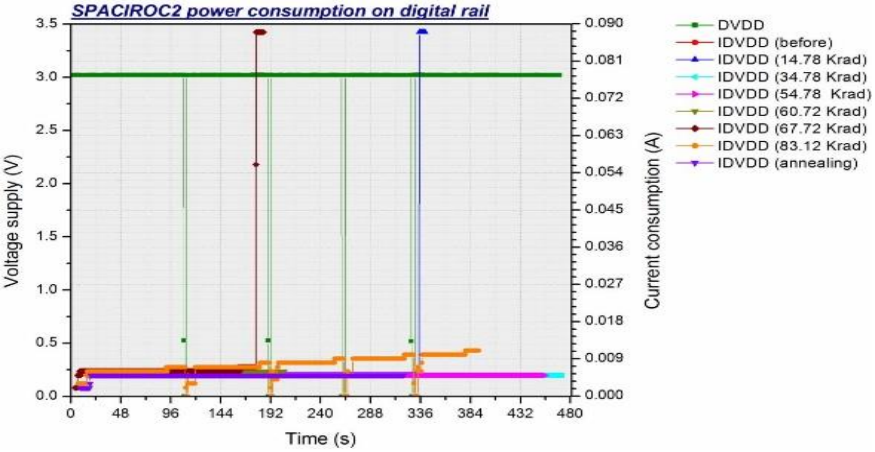

Figure 4-4 Digital current consumption for the third chip during irradiation.

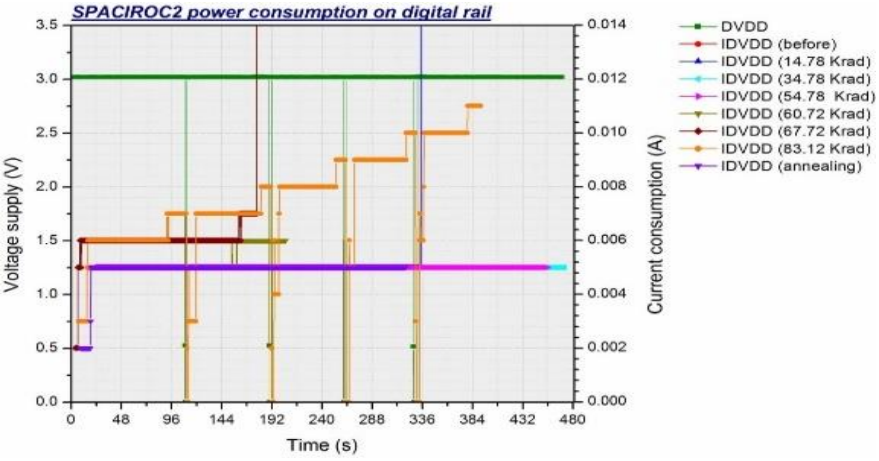

Figure 4-5 Zoom on digital current axis of the third chip under irradiation.

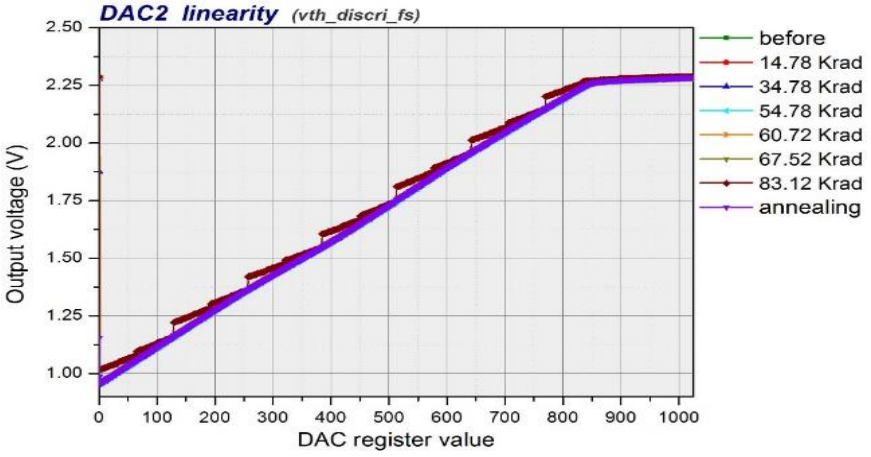

Figure 4-6 The DAC2 linearity test for third chip after each dose.

No voltage variation in the DAC2 output was observed before during irradiation, however DAC2 lost the linearity of its response during the last beam exposure when the TID between

67.72 and 83.12 krad was absorbed by the DUT - see figure 4-6. Through annealing the DAC2 linearity curves were recovered.

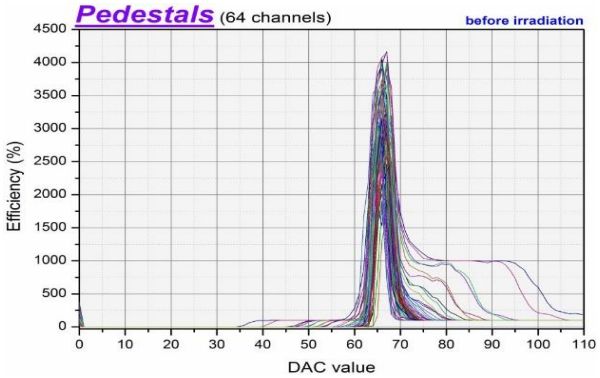

Figure 4-7 Pedestals curves of the third chip before irradiation.

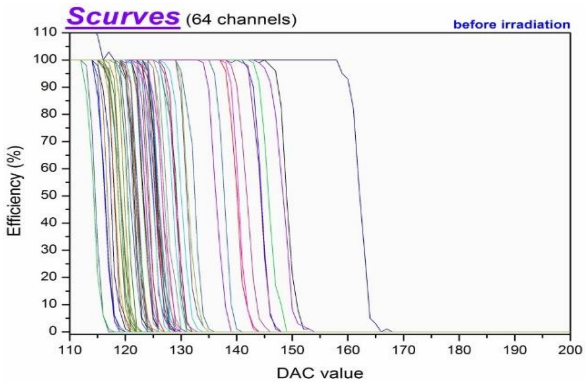

Figure 4-8 Efficiency curves of the third chip before irradiation.

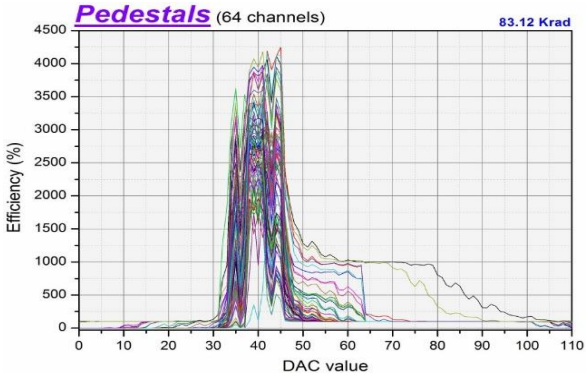

Figure 4-9 Pedestals curves of the third chip after 83.12 krad.

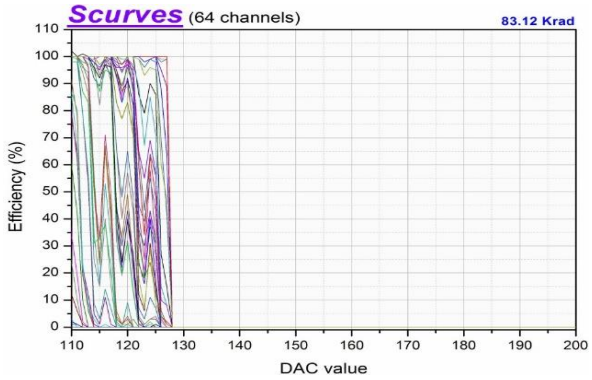

Figure 4-10 Efficiency curves of the third chip after 83.12 krad.

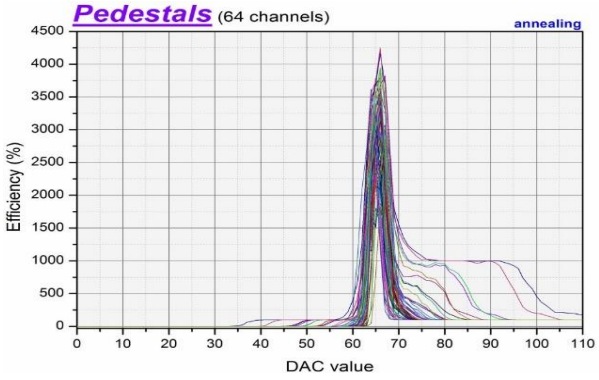

Figure 4-11 Pedestals curves of the third chip after annealing.

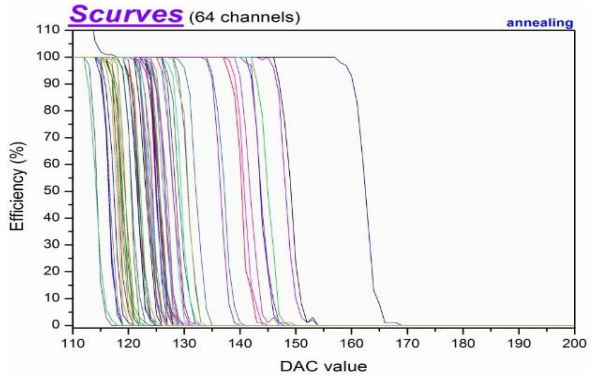

Figure 4-12 Efficiency curves of the third chip after annealing.

The trigger efficiency curves were measured for an input charge of 150 fC, thus 1 p-e. The pedestal curves overran the Scurves during the deposition of the last dose, see figure 4-9 and 4-10, up to the 83.12 krad TID corresponding to the loss of DAC2 response linearity. After annealing the efficiency curves in figures 4-12 showed negligible to no variations from their shapes and values measured before irradiation, see figure 4-8. As well as for the pedestals curves figure 4-7 and 4-11.

I did a close analysis for the trigger efficiency curve on each of the DUTs channels. For this purpose, a Python script was developed to check if the individual channels of the irradiated chip samples changed their position, form or slope from dose to dose. As general observation, on either chips the pedestal curves and Scurves significantly shifts after 60 krad TID or equivalently the trigger efficiency is getting worse. In all channels investigated, the pedestals curves changed their form and position after the accumulated TID exceeded the above value.

4.3 Conclusions and originality

Expertise from the SPACIROC2 development group allowed me to better understand the chip operation and to propose a monitoring strategy. Moreover, experience gained irradiating the MAROC3 chip in X-ray beam was useful to improve the automatic test bench for the chip parameter online monitoring during radiation hardness qualification of SPACIROC2. Thus, the newly designed test bench meets the requirements, but also for next versions of these chips.

I had with my group the opportunity to perform the very first characterisation of the SPACIROC2 radiation tolerance. The results obtained during the irradiation using a proton beam of 200 MeV mean energy was subsequently discussed with the OmegaMicro working group, special attention being given to the digital block of the chip. Planned to take data for 4-5 years in the hostile environment of Low Earth Orbit (LEO), the electronics on board of JEM-EUSO space observatory will be exposed to about 0.1 krad TID per year. Considering that the proton beam had a flux of about 1.089×10^9 particles /cm^{2}s, the annealing is expected to overcome the rate of radiation induced effects for the much lower particle rates registered in LEO environment. Therefore, the SPACIROC2 chip proves to be a viable technological choice since it can withstand up to 60 krad TID. On the other hand, this prototype version of SPACIROC was found not to satisfy the radiation hardness requirements imposed by experiments at the LHC where doses and particle rates would exceed the levels tolerated by the chip electronics.

The relative complex digital part of the SPACIROC2 prove to be prone to radiation effects causing malfunction. This block of the chip will be carefully investigated in future tests, for instance the linearity of all four built-in DACs will be measured. Also, the DACs linearity curves saturation at the end of output voltage range it will be fixed by modifying the external bias resistor. The SELs associated with high current states on the digital supply rail which was observed for two out of three tested chip is an important cause of concern. We postulate that these latch-ups probably appear from disturbances of the electronic structures produced by heavier secondary (Si, Ge or metallic) ions generated. Significant contribution to the high current states could also come from SEU/MBU affecting the chip configuration registers. For upcoming radiation hardness tests, a procedure was developed to readback the configuration registers which would then reveal when corruption due to SEU/MBU occurs. Both assumptions will be investigated during irradiation of the SPACIROC2 chips in beams of various heavy ion species. Thus, for this proton irradiation test the computed SEL cross-section is $0.78 \cdot 10^{-12}$ cm^2 with 54% uncertainty. In the cosmic environment, such heavy ions have LET values ranging from 0.01 to 40 MeV cm^2/mg. On this occasion, the chip vulnerability to catastrophic SEE will be explored.

5. Field Programmable Gate Array for High Energy Physics experiments

The design of a newly RICH photodetection system envisages new digital boards for photodetection elementary cells which will be implemented around a commercial base-line solution like SRAM FPGA. As a backup alternative, the antifuse FPGA is being considered. The Xilinx 7 series devices are available in four state-of-the-art FPGA families implemented in a 28 nm high-k metal gate (HKMG) technology. The KINTEX-7 FPGA family was selected as an attractive solution for the digital board given careful considerations to: the cost-performance balance and the input/output capability which matches those of the read-out electronic system from the upgraded elementary cell. With support and expertise from RICH Upgrade working group, I put forward the test bench architecture presented in figure 5-1. Thus, the testing procedure was worked out in close collaborating with the Cambridge LHCb Group.

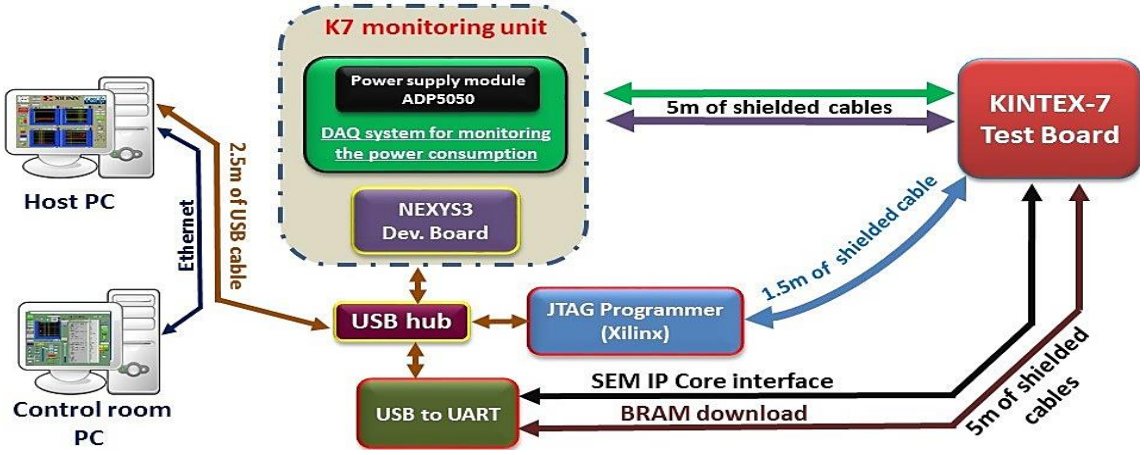

Figure 5-1 Test bench for a KINTEX-7 chip online monitoring under radiation.

An entire test architecture is developed around the KINTEX-7 chip which is mounted on the test board together with minimal chip-external electronic components. These fulfil a set of minimal requirements for the FPGA basic operation, while its reprograming is done through the standalone XILINX JTAG programmer connected over a ribbon cable at the FPGA board. The DUT power supply has four rails which are continuously monitored by the DAQ system. Further, the status of firmware written on the DUT is continuously checked with the help of a NEXYS3 development board housing a SPARTAN-6 FPGA. All data are transmitted from NEXYS3, JTAG programmer and DAQ system to the host PC situated in the irradiation room, over USB links.

Exploring the radiation hardness of such complex devices as the FPGAs relies heavily on the firmware. Our group adopted a straightforward solution to instantiate only those KINTEX-7 logic elements desired to be tested at a given time under radiation. Figure 5-2 shows the general architecture of a firmware for the FPGA test board within the irradiation test bench. In KINTEX-7 FPGA, the configuration memory (CRAM) is the largest memory which is embedded in the device. Our DUT has in total 18884576 bits of CRAM used to customise the device logic function in the application. Even a single bit flipped by radiation in CRAM might have a severe and potentially very harmful effect on the device operation and in extreme cases could cause a failure in the entire system by burnout. The SEU occurrence in CRAM can lead to a mismatch in the FPGA logic fabric by changing the CLB function or switching the routing network topology.

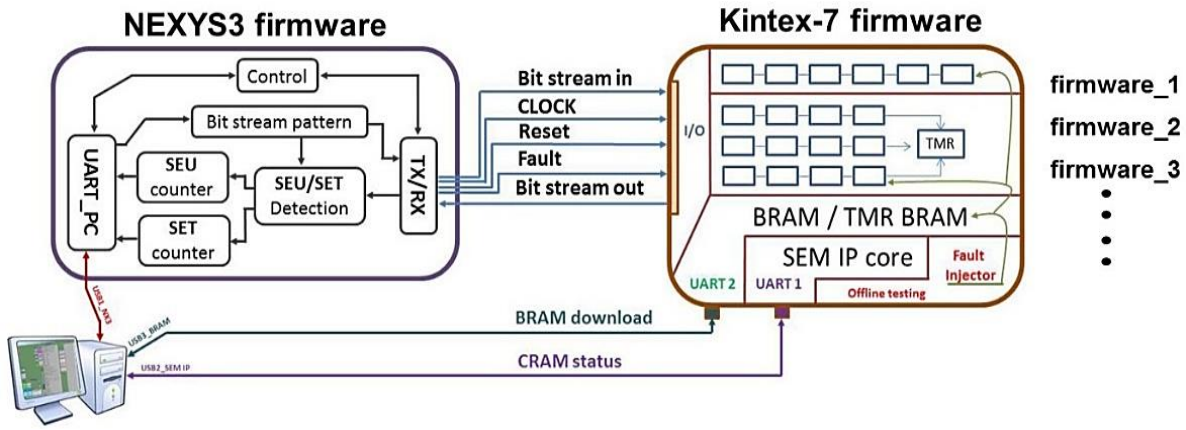

Figure 5-2 The firmware layouts for NEXUS3 and KINTEX-7 irradiation, including a SEM IP core for the CRAM's scrubbing.

Thus, the use of Soft Error Mitigation (SEM) Core from XILINX was considered as an internal scrubbing solution for the KINTEX-7 FPGA. This core can be put in an idle state and through its UART link or the SPI interface it allows to inject errors at specific CRAM bit addresses. So, the users have the possibility of simulating an SEU effect with the developed firmware in order to see how the device behaves.

5.1 Heavy ions irradiation of KINTEX-7

The first testing was undertaken at the SIRAD facility from INFN Legnaro National Laboratory, Padova, Italy. For this heavy-ion irradiation facility there are available a wide variety of ion species with a LET value spamming from 0.02 MeV cm^2/mg and 4390 µm penetration depth to 81.7 MeV cm^2/mg and 23.4 µm range in silicon. Figure 5-3 presents the irradiation room at SIRAD with the beam line and vacuum vessel in open position giving access to the sample holder. The flux of ions in beam can be modified between 10^5 and $5x10^8$ ions/cm^2/s.

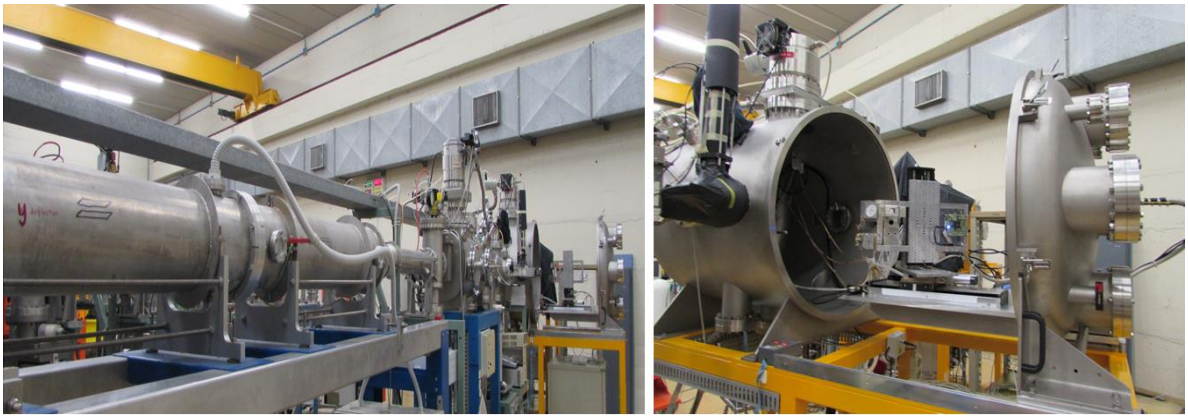

Figure 5-3 Legnaro Tandem- XTU accelerator beam pipe and the KINTEX-7 test board installed within the vacuum vessel.

The second irradiation test was made possible through a AIDA2020 EU program, carried out at the Cyclotron Resource Center in Louvain-la-Neuve, Universite Catholique de Louvain Belgium (UCL). The Heavy Ion Irradiation Facility (HIF) makes available a wide variety of

ion species with LET ranging from 0.4 to 56 MeV/(mg/cm^2) and this only for its high penetration cocktail beam. Concerning the beam, it has a maximum diameter of 25 mm, and ±10% homogeneity, while the flux can be modified from a few ions/ cm^{2}s to about 10^5 ions/cm^{2}s. Figure 5-4 presents the irradiation chambers plus the KINTEX-7 test board mounted on the sample holder and seen through a transparent aperture on the vessel metallic body.

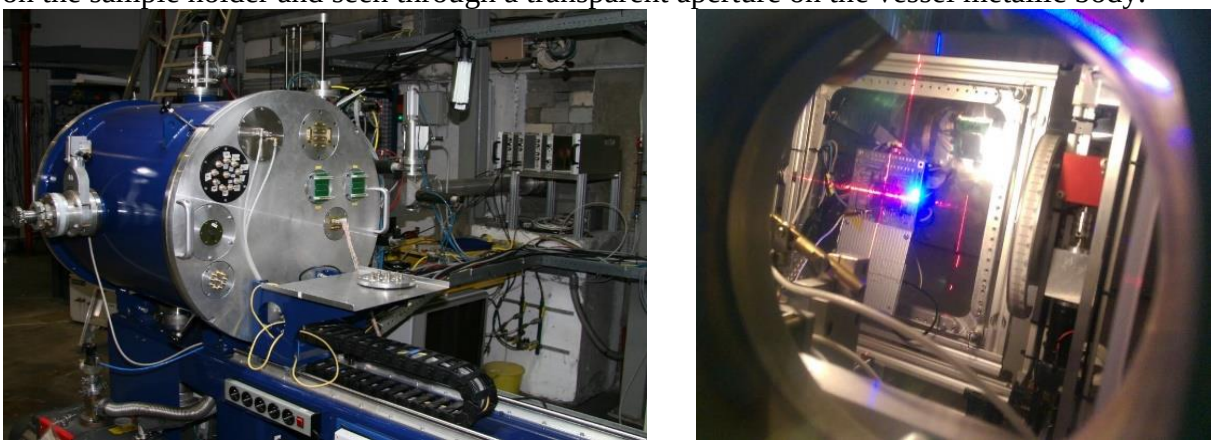

Figure 5-4 The HIF vacuum chamber in close position and the inside view during laser alignment of the DUT.

The aim of the first irradiation test performed at SIRAD was to inquire how harmful are the radiation induced effects on an FPGA when its CRAM has no scrubbing and error mitigation. Two types of ions have been used during irradiation Oxygen ^{18}O at 108 MeV with the LET 3.197 MeV cm^2/mg (TRIM estimate) and Florine ^{19}F at 122 MeV with the LET 3.67 MeV cm^2/mg (LNL estimate with is for surface) or 3.899 MeV cm^2/mg (TRIM estimate is given for bulk). The firmware was set to occupy just 40% of the FPGA logic resources.

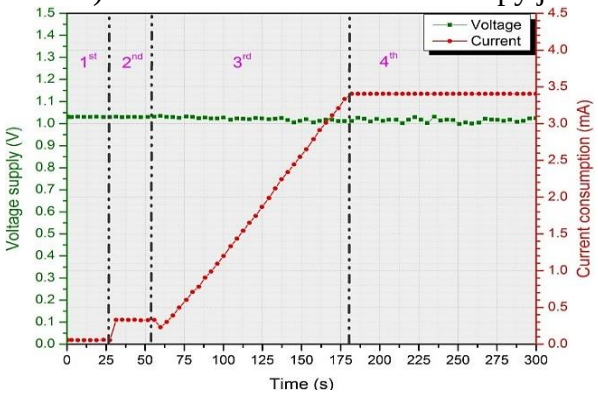

Figure 5-5 High current state on core and BRAM supply rail during a ^{19}F ions test, run away SEU accumulation.

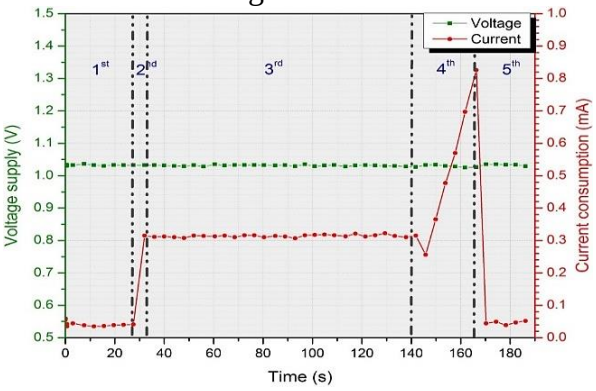

Figure 5-6 DUT unknown state revealed by a core current under ^{19}F ions action, SEFI.

As example, one of the tests performed under a ^{19}F ion beam showed that the current increases gradually because of the accumulation of SEUs in the CRAM. So, unwanted and parasitic logic elements within the FPGA were induced by the CRAM corruption, see figure 5-5. Also, behaviour typically of SEFI phenomena was observed on the DUT, see figure 5-6, and the FPGA core and the BRAM current consumption doubles in less than 15 seconds followed by quickly decrease to the level were the device is unprogrammed. This time the firmware occupancy was close to 100%.

During heavy ions irradiation test it was recorded a current jump with a signature corresponding to the micro latch-up events from literature, and the current was detected on the

1.8V power rail as in literature, too. Cumulated fluency on DUT was $7.56 \cdot 10^5$ ions/cm^2. Figure 5-7 presents a current increasing in steps of approximately 100 mA, modifications which are not removable through a configuration scrubbing or blind scrubbing, but only by power cycling the device. The power dissipation on FPGA lead to its dice temperature increasing up to 70 ^{0}C, see figure 5-8. Similar behaviour is described also in literature for another FPGA from the KINTEX-7 family.

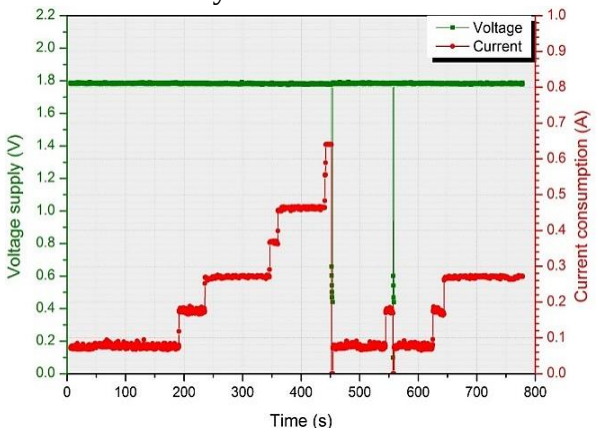

Figure 5-7 SEL induced by ions with a LET of 15.56 MeV cm^2/mg in a 1.8 V power rail.

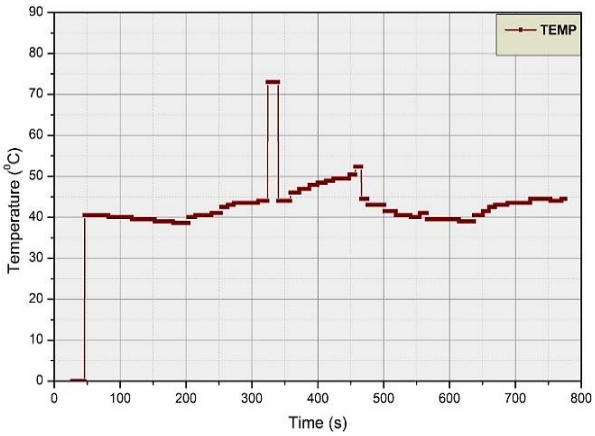

Figure 5-8 The DUT dice temperature during irradiation with $^{40}Ar^{12+}$.

We continue to investigate the KINTEX-7 susceptibility to SEL using species of ions with a higher LET. Therefore, the next test was done using $^{58}Ni^{18+}$ ions at 582 MeV and LET of 20.4 MeV cm^2/mg. The final test was carried out with a 769 MeV beam of $^{84}Kr^{25+}$ ions, species having a LET of 32.4 MeV cm^2/mg. The beam flux was 10^3 ions/cm^2/s and the total fluency was 9.11 times 10^5 ions/cm^2. This time several high current states have been recorded and this time not only in 1.8V power rail, but also in 1.5 V power rail and 3.3 V power rail. By power cycling the FPGA we confirmed the SEL occurrence on each above power rail excepting the core power rail.

5.2 Irradiation test with 200 MeV prtotons

A compulsory pass or fail test is the TID one with the threshold set at 200 krad in case of the RICH subdetectors. For this purpose, we have accessed the PIF/proton-facility at PSI where we have tested the SPACIROC2 chip, too. The irradiation was carried out with a proton beam at 200 MeV and a flux ranging from 10^7 up to 10^9 particles/cm^2/s. Three FPGA chips were irradiated subsequently each up to 500 krad TID-equivalent in Silicon with accumulated fluency per device at around 10^{10} and 10^{12} protons/cm^2. Even though, the dose has exceeded two and half times the nominal one, 200 krad expected for the in LHCb-RICH Upgrade phase worst case scenario, we have seen no Latch-Up and the device after reprogramming was recovering completely from SEUs. Moreover, no permanent effects were seen on the tested devices, no increase in currents or voltage fluctuation. Again, a high SEU rate in CRAM was recorded for the proton test, but at lower rate than for heavy ions irradiation, which is expected. Post irradiation tests did not show any sign of cumulative effects that might compromise the KINTEX-7 device.

5.3 Conclusions and originality

The radiation qualification study of our low-end KINTEX-7 FPGA is made from the perspective and constrains dictated by the expected mix-field radiation environment within the LHCb detector for 50 fb^{-1}. An automatic test bench was design and implemented to record electrical and software parameters of DUT during the evaluation tests. The KINTEX-7 board design was kept as simple as possible. In this way, it was ensured that the radiation tolerance measurements are not compromised by the misbehaviour of other non-radiation hard semiconductor devices. Moreover, the test board respects the outlines of digital board requirements such as no external flash memory for the FPGA. Data are gathered in ASCII files for later analysis. The FPGA power consumption on the main four supply rails is measured at each 50 ms, while the SEM IP status report is continuously stored. Safety constrains on additional electronic equipment used for the FPGA monitoring pushed the setup to its limits. As example for proton testing, the monitoring unit was placed at 5 m away from DUT, while the sampled data was transmitted via another 5 m of USB cable to the host PC and further over Ethernet to the PC from the control room.

The heavy ions tests carried out cover a few crucial aspects regarding the KINTEX-7 tolerance against SEEs. More tests and beam time is required to finalise a thorough study on this DUT and it envisage radiation tolerance measurements of other important FPGA built-in logic elements like BRAM, SLR32 and I/O banks. So far, we confirmed what other literature sources present about micro latch-up occurrence at a LET right above 15 MeV cm^2/mg for other not space grade KINTEX-7 FPGA. The CRAM study under heavy ions without error mitigation and without scrubbing solution allowed us to become aware about several effects that might occurs even when a single bit is flipped, and about the SEU cumulative effect in absence of blind scrubbing. The SEM IP core proved a good solution to do a quick and cost-effective investigation into the FPGA configuration and the potential corruption effects. Throughout its means, we had the chance to experience how the FPGA behaves when the CRAM is corrupted deliberately by injecting errors at specific memory location. Unfortunately, the build-in FPGA error mitigation and the scrubbing efficiency in repair or enhanced-repair mode are dropping fast to 0% when the beam has a very high flux or the particles have a high LET. We took into consideration the use SEM IP core in replace mode with an external flash memory connected to it, this will allow us to have a much better CRAM error mitigation efficiency, though new test for flash memory radiation hardness have to be done.

The proton irradiation test was a complete surprise since the KINTEX-7 withstood to 500 krad TID without notable failures due to cumulative effects (SEU rates are very high though). From what the literature mentioned, no other KINTEX-7 FPGA was irradiated to a so high TID level. However, the unexpected rate of SEU induced by protons in CRAM remains a very big concern. There, the proton beam fluxes between 10^7 up to 10^9 particles/cm^2/s was used. No kind of cumulative effects were observed in the accomplished tests in post irradiation phase.

Thorough study on KINTEX-7 radiation tolerance is ongoing to better understand how the device behaves and what might compromise its usage in the digital boards for RICH sub-detectors photodetection system. If it will be decided that it is feasible to run these FPGA with some degree of reliability in the LHCb's mixt-radiation environment, then almost 3000 FPGAs will be acquired by LHCb for sub-detectors reconstruction in the LS2 of LHC – Upgrade Phase.

Conclusions and personal contributions

The LHCb-Romanian group offers its support towards building the new Upgraded LHCb detector. This is done by being, e.g. actively involved in Research and Development (R&D) Program of LHCb with focus on the radiation hardness qualification campaign dedicated to the new semiconductor devices. These ICs are considered for the RICH sub-detectors photodetection read-out system. As member of the group, my main involvement so far has been to contribute, in the context of radiation hardness studies, to: MAROC3 front-end ASIC irradiation and data analysis and the testing of low-end FPGA from the KINTEX7 family in LHC conditions. The final goal of these tests was to extrapolate based on the gathered data if these IC devices can have a reliable running for given period in the nominal conditions of mixt-field radiation environment, temperature and magnetic field fluctuations estimated to be inside the LHCb detector for the Upgraded Phase (luminosity 50 fb^{-1}).

Specially developed for the JEM-EUSO telescope, the SPACIROC2 is the second ASIC studied by our group, and the radiation hardness to ionizing radiations was mapped for ESA-ISS space-like conditions. This ASIC prototype version serves also as a blueprint of the next generation of MAROCs. The radiation hardness qualification of these three devices depend heavily on the data collected during the irradiation tests. For each of them a list of quality-parameters was established for online monitoring. Using custom test benches presented in the previous chapters, these parameters are measured continuously and complementary to a set of offline parameters which are measured after and before beam/irradiation. Among the contributions made to evaluate the radiation tolerance of the three chips, this present section seeks to highlight the experimental, practical and theoretical personal contributions.

I. Experimental contributions

I was successful in establishing well defined strategies to test the MAROC3, SPACIROC2 and KINTEX7 using different radiation sources. This was made possible mainly due to the collaboration with the LAL-OmegaMICRO chip design team and the other foreign groups partners in LHCb. Since the testing boards provided by OmegaMICRO for MAROC3 and SPACIROC2 were not designed to be used in radiation environments, special precaution had to be taken regarding the test setup to allow exposing only the DUT to the beam. A lead mask has been made to protect additional devices residing on the board near the DUT. Thus, for the KINTEX-7 we designed the test board exclusively to testing in order to be exposed to radiation, so no extra material in front of the board was needed. My contribution to the irradiation test benches design and implementation along with the testing procedure as well as to the data analysis are summarized in the following paragraphs.

After studying the MAROC3 architecture and test board, in addition doing extensive tests in normal conditions without special radiation or field conditions, I proposed a test bench architecture for MAROC evaluation under radiation. In agreement with the ASIC design team I drafted the list of parameters to be monitored. I started the design and implementation of the MAROC3 test bench in the following way:

- Firstly, I sketch the layout of an automatic test bench architecture around the NI USB6009 commercial DAQ system. This allowed to monitor online various parameters across the MAROC3 test board and to have a proper control over other parts of the test bench like the power supply to IC.
- Powering the MAROC3 test board on the irradiation site was possible with a custom made remote power supply, capable of delivering +6.5 V and -7.3 V. I designed this power

module to deliver up to 1.5 A on each of the two rails. Moreover, through the DAQ system it can be switched ON/OFF the output rail voltage, in order to do power cycling for the ASIC when it is needed.

- To pinpoint eventual SEUs that might prove as destructive as SEL, I brought my contribution to the current measurement circuits for MAROC3.
- For monitoring the heat dissipation in the MAROC3 chip under irradiation, I selected two type of sensors to be used in the temperature monitoring strategy. We have used the PT100 transducer mainly to monitor any changes in temperature for the bottom part of the PCB underneath ASIC, while for the MAROC3 dice surface, it was used the MLX90614 infrared temperature contactless sensor and I shielded the implemented circuit in 5 mm thick lead case against beam halo scattering. I have assembled the hardware part of the MXL90614 IR sensor including the processing unit base on a ATEMGA326 microcontroller.
- I have equipped the test bench with all the shielded cables required to complete the setup. Also, I studied and characterized the MAROC3's behaviour in normal condition of operation.
- The LabVIEW GUI used to control the test bench for MAROC3 was partial developed by me. Through this GUI, it was possible to record in ASCII files the reference/monitored parameters before the irradiation of each of the ASIC samples.
- Regarding the MAROC3 irradiation with X-ray, I was involved in the test bench installation on beam line, plus in the DUT monitoring over the testing period.
- I took part at the data analysis and I made the interpretation of all electrical parameters recoded during irradiation test and post irradiation.

SPACIROC2 inherited multiple elements from MAROC3's architecture. Because of their similarity, we had designed a new test bench that fulfils the monitoring requirements of both ASIC. This time the DAQ system of test bench was custom-made by us, all shortcomings of the commercial DAQ were avoided. My experimental contribution to SPACIROC2 chip radiation tolerance investigation is summarised below.

- The OmegaMICRO design team provided us the GERBER files for a PCB production and the SPACIROC2 test board schematic. I was in charge with sending the PCB to the foundry for manufacturing and after I assembled in the lab three SPACIROC2 test boards entirely, and test them to prove they were fully functional.
- Since the ASICs were mounted on the test boards via clamshell sockets, I have adapted it to the chip ceramic package to allow connections to the SPACIROC2 die. Further, using a microscope I have aligned each of the chip's pins with those of the socket.
- The test bench parts were design under my supervision and I participated in the monitoring unit assembly. In addition, I have equipped the setup with all the needed shielded cables.
- I had also a few contributions to the GUI development for the DAQ system and solid contribution to the SPACIROC2 characterisation before the irradiation procedure.
- Again, I took part in the test bench installation on proton beam line at PSI Institute in Switzerland, as well as in the monitoring procedure.
- The measured data have been carefully analysed and I added my contribution to the interpretation of electrical parameter changes.

The KINTEX7 FPGA represents the main electronic device to used on the future digital boards for the RICH sub-detector chains, at least in the present design. Testing its radiation hardness implies to access various irradiation facilities, plus an increased human and financial resources due to the complexity of the hardware as well as that of the software/firmware. Our contribution was to design and implement entirely the KINTEX7 FPGA test bench and boards in agreement with the indications suggested by the LHCb collaboration experts. The KINTEX-7 test board was designed to accommodate a minimal number of electronic components needed by the FPGA to have a at least a basic/simple user logic. The steps taken in the design and implementation of the test bench for the KINTEX7 radiation qualification were up to now was:

- To propose the architecture layouts for the FPGA test board, the power supply board, and the DAQ system. Each of these have been discussed in the LHCb Collaboration meetings and afterword approved for implementation.
- I had to supervise the schematic and the PCB design to all boards specially developed for the KINTEX-7 test bench.
- After the PCB arrived from the factory, I completely assembled 9 FPGA test boards out of which 4 are with thinned FPGA chips. For this I have used an IR-infrared reworking/reballing station. Same is true for the other 4 power supply boards assembled by me.
- The monitoring unit of the KINTEX-7 was implemented with my support, while the shielded cables needed for setup were installed by me.
- When the setup was complete, I got involved in the device testing and I coordinated the firmware development. In addition, I suggested several improvements to the GUI design and functionality. Overall, I had to debug the hardware problems occurring during the setup implementation up to its final version.
- I provided expertise for the SEM IP core use and I took part in the offline tests carried out in the laboratory.
- Regarding, the irradiation tests pursued at SIRAD Legnaro, HIF Louvain and PSI, with my colleagues, I had to install the setup at the facilities, and on the beam lines and I have attended to the device monitoring.
- Finally, I got involved in the laborious data analysing procedure for the KINTEX-7 irradiation. The device behaviour had to be explained by corroborating the electrical and software/firmware parameters recorded during these irradiation tests.

The irradiation qualification tests remain the only straightforward solution to inquire the radiation resilience of an integrated circuit. Despite been costly, time consuming and work-power demanding the irradiation tests provides crucial data based on which the device behaviour can be extrapolated for a certain radiation environment during many years. Up to now, the data gathered over multiple tests tends to maintain the interest of using in the LHC radiation environment the KINTEX-7 chips, though other solutions are being investigated due to the large measured SEU rate in these devices. More tests must be performed on the MAROC3 to better understand its radiation tolerance. On the other hand, the SPACIROC2 passed at limit the TID test, while the heavy ions irradiation will clarify the chip's immunity against SEEs. The KINTEX-7 is a promising solution for the digital board especially after successfully passing the TID test. No destructive SEE effects occurred on it during heavy ion testing. However, the high SEU rate in CRAM remain the main issue to be overcome through configuration scrubbing and error mitigation.

II. Theoretical contributions

I have done reports, periodically, on the MAROC3, SPACIROC2 and KINTEX7 evaluation status to the LHCb collaborators and to the LAL-OmegaMICRO group from École Polytechnique of Palaiseau Paris, France. This allowed me to beneficiate from their expertise in the fields of rad-hard testing and the dedicated microelectronics which is used for high-energy physics experiments. Often, the encountered problems had solutions found during these meetings. A list of talks is summarised in the following:

1. ***Data analysis for the SPACIROC2 proton irradiation***, LHCb-Romania, September 21st 2016, IFIN-HH, Magurele, Romania, available at: https://indico.cern.ch/event/570828/

- On this occasion, I discussed with the SPACIROC2 design team the preliminary result of chip irradiation at 200MeV protons. The ASIC's behaviour above 60Krad was interpreted closely.

2. ***Preliminary results of KINTEX-7 irradiation with heavy ions at Louvain***, RICH Upgrade Meeting, June 14th 2016, CERN, Geneva, Switzerland, available at: https://indico.cern.ch/event/540695/

- I put forward the preliminary results outcoming from heavy ion irradiation at Louvain where the threshold LET for a micro latch-up (SEL) has been measured.

3. ***KINTEX-7 FPGA radiation hardness studies, test bench, firmware, error mitigation & scrubbing***, LHCb Upgrade Electronics, February 11th 2016, CERN, Geneva, Switzerland, available at: https://indico.cern.ch/event/490512/

- In the current presentation, I outlined the preparation that has been done to test the KINTEX-7 under radiation by emphasis the firmware's developed, plus the internal CRAM scrubbing and mitigation solution with SEM IP.

4. ***Update on SPACIROC2 testing***, Omega MICRO designer team, November 19th 2015, Drahi-X Novation Center, Ecole Polytechnique, Paris, France.

- Here I presented to the LAL-OmegaMICRO group the test bench and monitoring strategy for SPACIROC2 proton irradiation.

5. ***Status and perspectives for KINTEX-7 irradiation***, Mini-meeting on irradiations for RICH Upgrade, July 8th 2015, CERN, Geneva, Switzerland available at: https://indico.cern.ch/event/406534/

- The irradiation plan along with the status of KINTEX-7 setup were presented in details.

6. ***Update on KINTEX-7 irradiation setup***, RICH meeting, June 8th 2015, CERN, Geneva, Switzerland available at: https://indico.cern.ch/event/399125/

- I presented the new features and improvements brought to the test bench architecture.

7. ***First prototype of KINTEX7 module designed for irradiation tests***, RICH Upgrade Testbeam Meeting, April 1st 2015, CERN, Geneva, Switzerland available at: https://indico.cern.ch/event/385716/

   - On this occasion, I introduced the functional version of the KINTEX-7 basic test bench for radiation hardness evaluation.

8. ***Irradiation of MAROC3 with X-Ray and the KINTEX7 PCB design***, Mini-meeting on Irradiations for RICH Upgrade, February 20th 2015 CERN, Geneva, Switzerland, available at: https://indico.cern.ch/event/374595/

   - Results have been shown from the testing of two MAROC3 chips to X-ray along with the preliminary KINTEX-7 test bench architecture.

9. ***Characterization of the MAROC 3 before irradiation***, RICH Upgrade Testbeam Meeting, July 23th 2014, CERN, Geneva, Switzerland, available at: https://indico.cern.ch/event/331717/

   - In this presentation, I proposed a test bench architecture for online monitoring of the MAROC3 during the irradiation process along with the final list of parameters selected to be monitored, as well as the testing procedure.

10 ***Multi Anode ReadOut Chip (pre-irradiation tests)***, RICH Upgrade Testbeam Meeting, June 11th 2014, CERN, Geneva, Switzerland, available at: https://indico.cern.ch/event/324199/

   - Here I made known a couple of issues that withstood against the MAROC3 characterisation in normal condition of running.

III. Results dissemination

The contribution added by the present thesis in the area of semiconductor devices radiation hardness qualification have been disseminated through journal publications and conferences. In the following are listed all the scientific contributions made.

A) Relevant papers for thesis topic:

[1] V. M. Placinta, **L. N. Cojocariu**, and C. Ravariu, "Test bench design for radiation tolerance of two ASIC's," *Accepted for publication in Romanian Journal of Physics (RJP)*, 2017, ISI journal with impact factor 1.398;

- The test bench architecture for measuring the radiation hardness of SPACIROC2 and MAROC3 has been published. Various cumulative and single event effects induce by radiation have been described along with the method to measured them.

[2] M. K. Baszczyk, M. Benettoni, **L. Cojocariu** et al, "Test of the photon detection system for the LHCb RICH Upgrade in a charged particle beam," *Journal of Instrumentation*, vol. 12, pp. P01012-P01012, 2017, DOI: 10.1088/1748-0221/12/01/p01012, ISI journal with impact factor 1.310;

- In this paper are presented the tests that have been made with a charged particle beam to a prototype version of an elementary cell populated with Hamamatsu R11265 MaPMT's connected to the CLARO front-end boards.

[3] **L. N. Cojocariu**, V. M. Placinta, and L. Dumitru, "Monitoring System for Testing the Radiation Hardness of a KINTEX-7 FPGA," *9th International Physics Conference of the Balkan Physical Union (Bpu-9),* vol. 1722, p. 140009, 2016, DOI: 10.1063/1.4944199, (ISI Proceeding);

- The test bench architecture for the KINTEX-7 radiation tolerance measurement has been published along with the first version of firmware layout used at SIRAD testing in Legnaro. Also, the SEL and the SEU impact in logic has been simulated.

[4] M. Prelipceanu, **L. Cojocariu**, A. Graur, and S. Schrader, "Analysis of thermally stimulated processes in new phenanthroline derivatives suitable for optoelectronic devices," *Journal of Physics: Conference Series,* vol. 585, p. 012011, 2015 DOI: 10.1088/1742-6596/585/1/012011, (ISI Proceeding);

- This study presents a compound suitable for optoelectronic devices that could have an application also in high-energy physics.

[5] R. Aaij, B. Adeva, **L. Cojocariu** et al, LHCb Collaboration, "Search for long-lived heavy charged particles using a ring imaging Cherenkov technique at LHCb," *European Physical Journal C,* vol. 75, Dec 2015, DOI: 10.1140/epjc/s10052-015-3809-7, ISI journal with impact factor 4.912;

- Here is published a detailed investigation on the RICH sub-detectors capability of distinguish from muons the heavy and slow-moving particles. The study is made for some proton-proton collisions at 7TeV and 8TeV centre of mass energy.

[6] R. Aaij, B. Adeva, **L. Cojocariu** et al, LHCb Collaboration, "LHCb detector performance," *International Journal of Modern Physics A,* vol. 30, Mar 10 2015, DOI: 10.1142/s0217751x15300227, ISI journal with impact factor 2.373.

- Based on data gathered from 2010 to 2012, the current paper amid to evaluate the LHCb machine performance by a closely approach on each sub-detector, including RICH. The results emphasise the LHCb detector role for introspecting matter and antimatter building blocks.

B) Conferences participation

1. **L.N. Cojocariu**, F. Maciuc, V.M. Placinta, "*Experimental study on Soft Error Mitigation Core (SEM IP) efficiency*", Workshop on Sensors and High Energy Physics (SHEP 2016), Stefan Cel Mare University of Suceava (USV), Suceava, Romania, 21 – 22 October 2016.
2. V.M. Placinta, **L.N. Cojocariu**, "*Test bench for ASIC radiation hardness evaluation*", Workshop on Sensors and High Energy Physics (SHEP 2016), Stefan Cel Mare University of Suceava (USV), Suceava, Romania, 21 – 22 October 2016.
3. **L.N. Cojocariu**, V.M. Placinta, "*Designing and implementing test benches for radiation hardness qualifications of readout electronics from LHCb RICH photodectors*", The 15th International Balkan Workshop on Applied Physics (IBWAP),

July 2-4 2015, Ovidius University of Constanta, Romania, IBWAP Book of abstracts, pp. 103-104.

4. V.M. Placinta, **L.N. Cojocariu**, ”*Practical test bench used for testing Photomultiplier Tubes, type MaPMT*”, The 15th International Balkan Workshop on Applied Physics (IBWAP), July 2-4, 2015, Ovidius University of Constanta, Romania, IBWAP Book of abstracts, pp. 115.

C) Other papers in the field of applied electronics

[1] **L. N. Cojocariu** and V. Popa, "Design of a multi-input-multiple-output visible light communication system for transport infrastructure to vehicle communication," *IEEE Xplore, International Conference on Development and Application Systems (DAS)*" pp. 93-96, 2014, DOI: 10.1109/daas.2014.6842435;

[2] M. Prelipceanu, **L. N. Cojocariu**, and A. Graur, "Surface investigations of vacuum Teflon thin films deposited on different materials suitable for medical applications and optoelectronics," *IEEE Xplore, E-Health and Bioengineering Conference (EHB)*, pp. 1-4, 2013, DOI: 10.1109/ehb.2013.6707421.

[3] **L. N. Cojocariu**, M. Dimian, and M. Prelipceanu, "Developing a wireless electrocardiography device for mobile and at-home healthcare applications," *IEEE Xplore, E-Health and Bioengineering Conference (EHB)*, pp. 1-4, 2013, DOI: 10.1109/ehb.2013.6707400.

D) Papers as member of the LHCb Collaboration authors list

Over 100 papers published in journals with high impact factor.